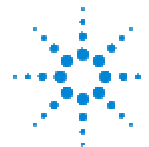


Andreas Olenyi
SOC-COE Application Consultant
27 March, 2001

Testing High-Speed HyperTransport Interfaces on Agilent 93000 SOC



Agilent Technologies

Content

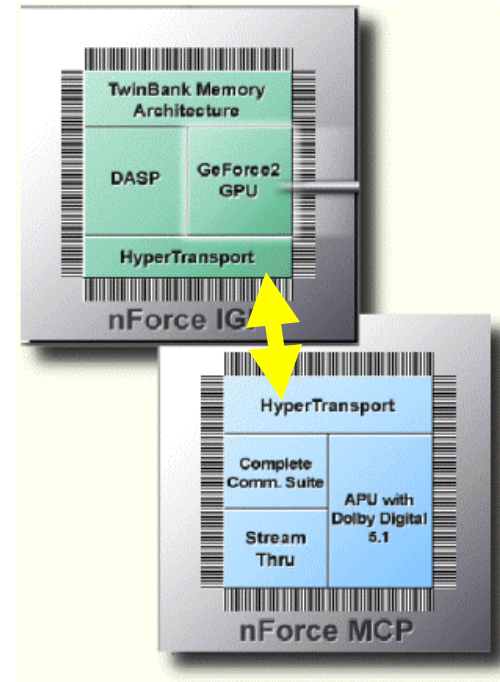
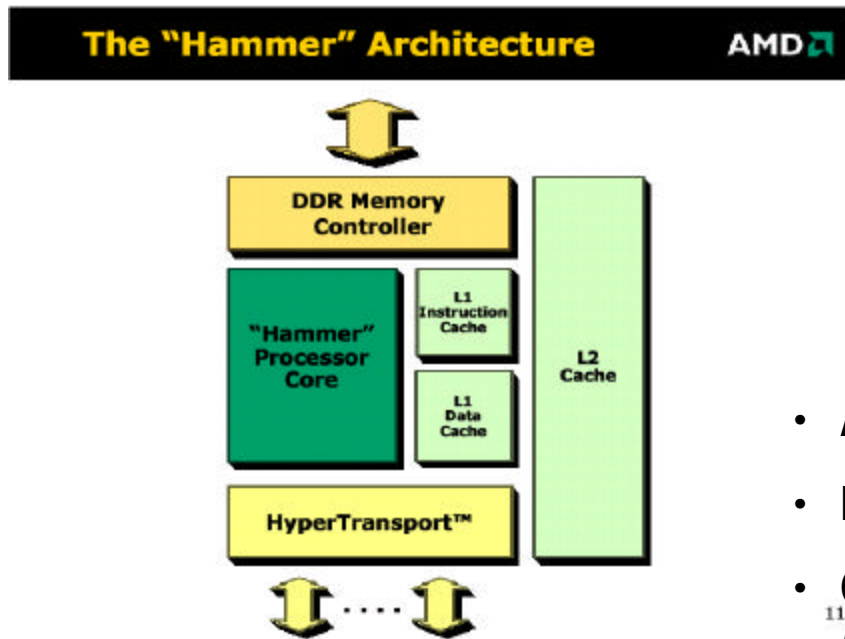
- HyperTransport Overview
- HyperTransport Tests & Challenges
- High-Speed Source Synchronous Test
- Summary and Q&A



HyperTransport Technology Overview



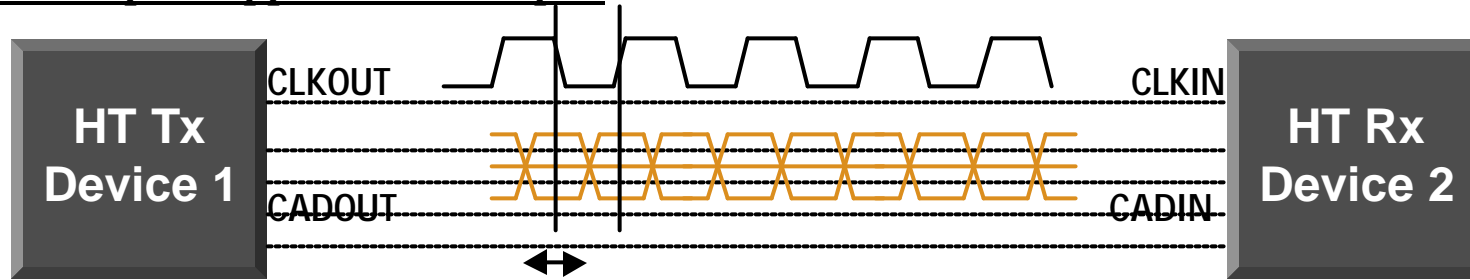
- Originally, HyperTransport was introduced by AMD
- Designed as high bandwidth solution for their next generation of Microprocessors.



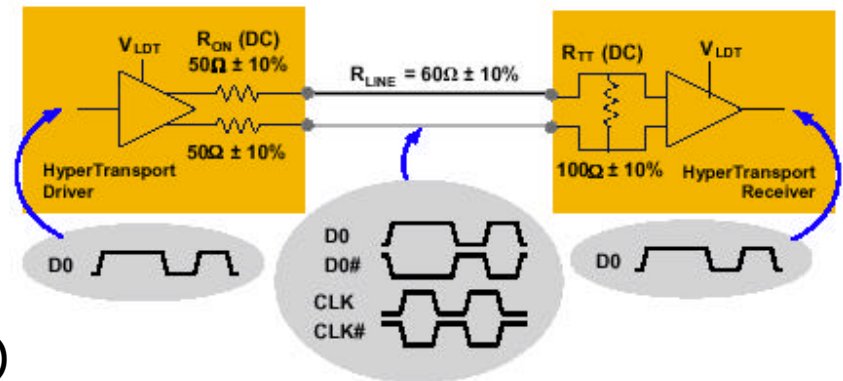
- A HyperTransport consortium was founded
- Meanwhile, many companies has joined
- Companies from different market segments (Transmeta, SUN, Cisco, PMC-Sierra, Broadcom)

What is HyperTransport?

HyperTransport Application example:



- Scalable I/O bus for high-speed operation
 - Bus Width: 2, 4, 8, 16, 32
 - Speed: 400Mbit ... 1.6 Gbit
- Designed for chip-to-chip link ('in the box')
- Differential, LVDS type signaling
 - Device Swing: Typ: 600 mV
 - Common Mode voltage: Typ: 600 mV
- Unidirectional bus (dedicated TX and RX lines)
 - 100 Ohm Cross Termination
 - 50 Ohm Driver Output Impedance



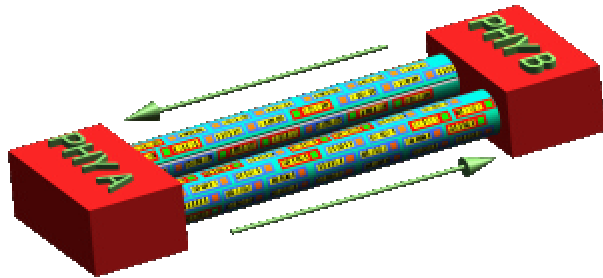
List of Different HyperTransport Parameters

	<i>PARAMETER</i>	<i>DESCRIPTION</i>	<i>TESTED with 93K/P800</i>	<i>TESTED with NP1700</i>
Level:	Vod	Differential Output Voltage	YES	YES
	Vocm	Output common-mode voltage	YES	YES
	Vid	Differential Input Voltage	YES	YES
	Vicm	Input common-mode voltage	YES	YES
Impedance:	Rtt	Differential Input Impedance	YES	YES
	Ron	Driver Output Impedance	YES	YES
Timing:	Tbit	Bit Time 400 Mbps	YES	YES
		800 Mbps	YES	YES
		1.6 Gbps	-	YES
	Tcadv	Transmitter output Clock/Data skew	YES	YES
			YES	YES
	Tsu	Receiver input setup time	YES	YES
	Tdh	Receiver input hold time	YES	YES
Tpllerror	PLL long term phase error	-	YES	
:	:			
:	:			

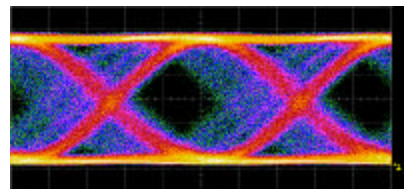
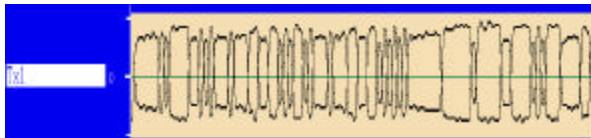
New Tester Capabilities



HyperTransport Test Challenges



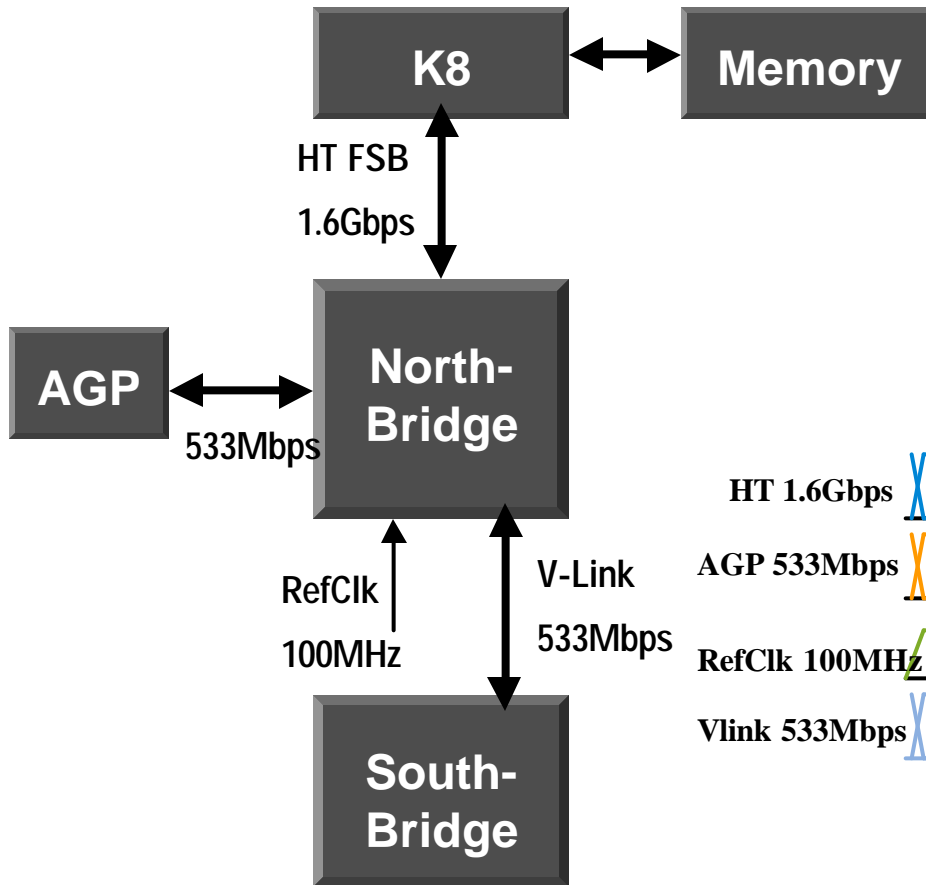
LVDS!



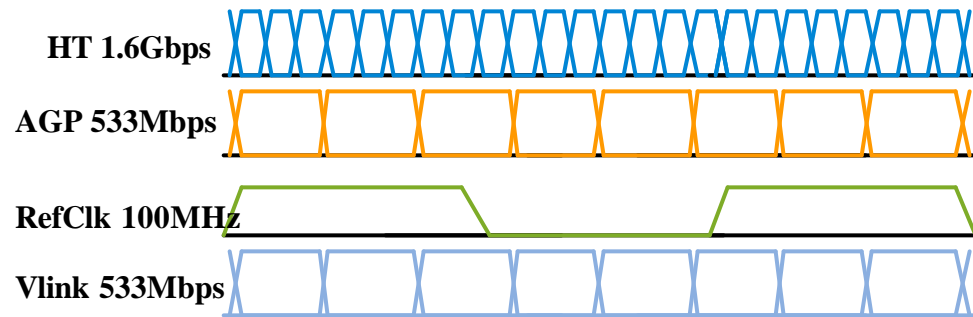
Source Sync!

- High Speed Data Rates up to 1.6 Gbit/s require Highest Speed and Accuracy
- Low Swing Differential Signals (DC/AC measurements)
- Debug & Characterize your High Speed Interface to bring your Device fast into production
- Source Synchronous bus interface

Application Example: North-Bridge Chip



North-Bridge Timing:



Application Example: North-Bridge Timing

Timing

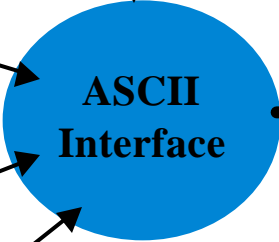
```
#PINS timing_apprx_20
Test 0 828 [rm]
dl_offset 0.0 [rm]
#FUNCTIONS timing_apprx_20
comp_edge = 0.0
dl_offset = dl_offset + tstr/3
# Definition of device cycle x8_1_dvc
#
DVC x8_1_dvc
period = tstr
#MODE ONLY STATE
DVS AGP-CLK+ AGP-CLK- SB-CLK+ SB-CLK-
0 0.0
1 1.0
#PINS AGP-DATA SB-DATA
0 0.0
1 1.0
L 1.0 L.comp_edge
H 1.0 H.comp_edge
#PINS FSB-CTLIN+ FSB-CLKIN+ FSB-CADIN+ FSB-CTLIN- FSB-CLKIN- FSB-CADIN-
0 0:dl_offset
1 1:dl_offset
#PINS FSB-CTLOUT+ FSB-CLKOUT+ FSB-CADOUT+ FSB-CTLOUT- FSB-CLKOUT- FSB-CADOUT-
L 1.0 L.xt_offset
H 1.0 H.xt_offset
```

Configuration

```
x8_PLATFORM P800
x8_DIR_FILE
dir_dir /tmp
hw_dir /hwf
x8c_dir /x8c
x8s_dir /x8s
single_binary_pattern_dir ./x8c/x8s/x8s_binary_pattern
p800DirFile ./x8c/x8s/x8s_p800DirFile
p800DirFile ./x8c/x8s/x8s_p800DirFile
x8c_dir ./x8c/x8s/x8s_dir
x8s_dir ./x8c/x8s/x8s_dir
x8_PLATFORM -AL
x8_PLATFORM -AL
#FUNCTIONS
Name type title context offset short equations | speed | anr_file | (hw_dir,dir_dir)
random_20 MAX 800 differential 0 0 timing_apprx_20 timing_apprx_20 x8_random_20 (x8_1_dvc SB_1) (x8_1_dvc SB_1)
```

Vectors

```
#PINS AGP-CLK+ AGP-CLK- SB-CLK+ SB-CLK- SB-DATA
#PINS FSB-CTLIN+ FSB-CLKIN+ FSB-CADIN+ FSB-CTLIN- FSB-CLKIN- FSB-CADIN-
#PINS FSB-CTLOUT+ FSB-CLKOUT+ FSB-CADOUT+ FSB-CTLOUT- FSB-CLKOUT- FSB-CADOUT-
#MODE ONLY STATE
#FUNCTIONS
```



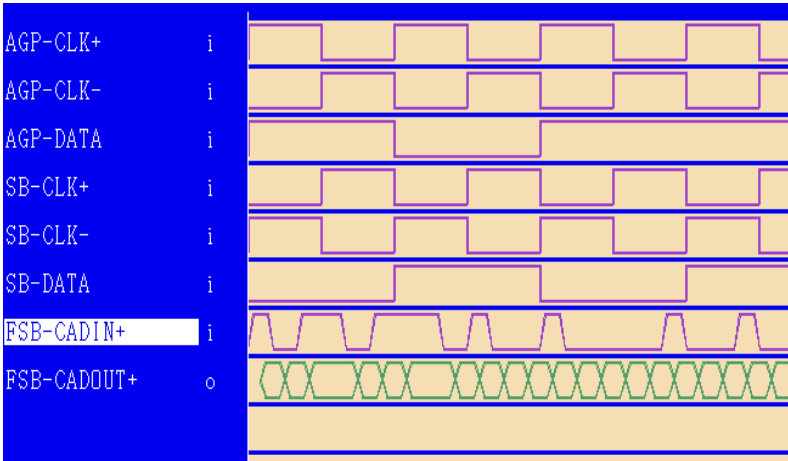
Combinations

```
# Definition of combination rules for x8_1_dvc
#
DDC x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc
PINS AGP-CLK+ AGP-CLK- SB-CLK+ SB-CLK-
[01] . . [01] . . [01] .

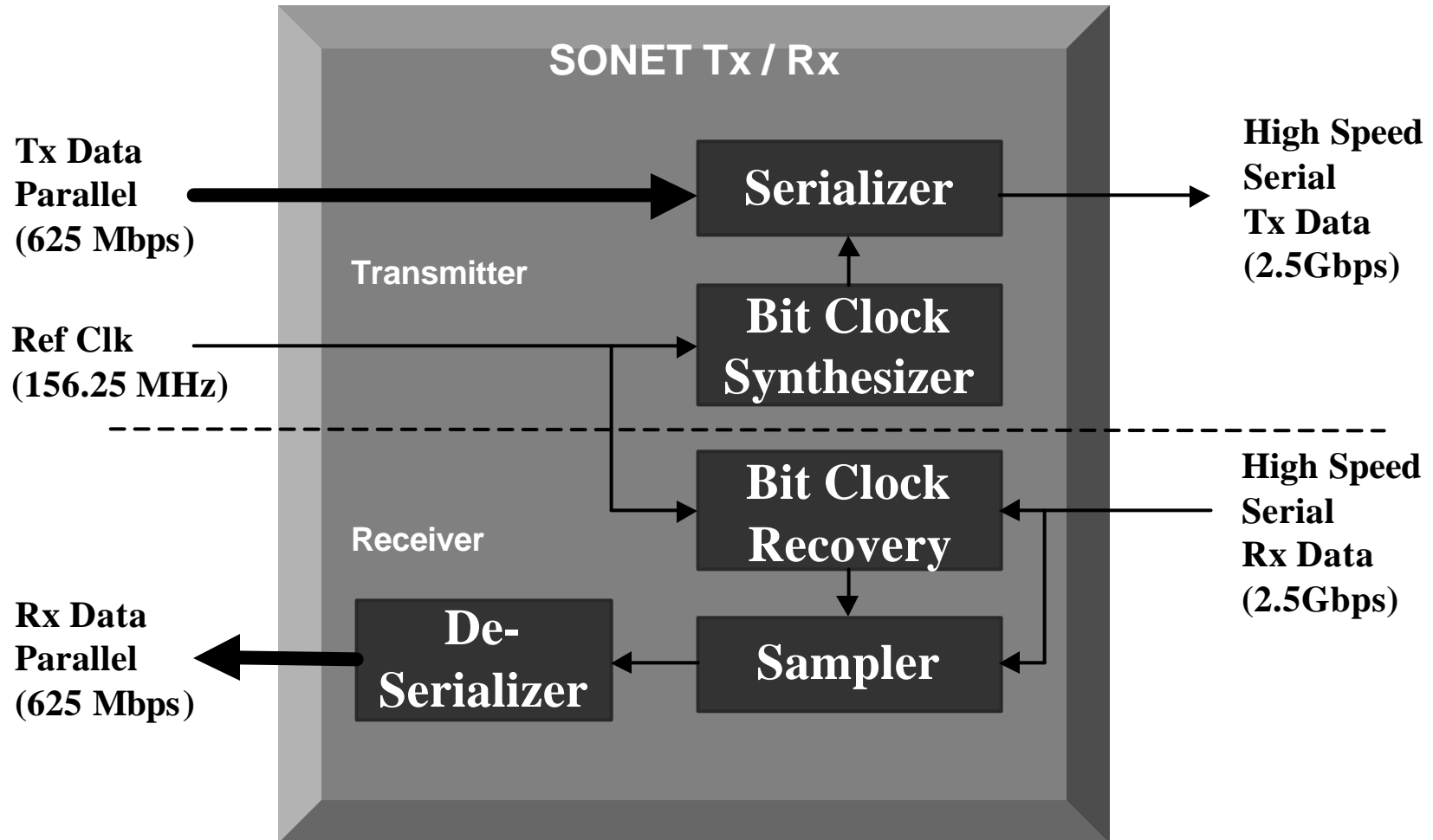
PINS AGP-DATA SB-DATA
[01] . . [01] . . [01] .
[LHX] . . [LHX] . . [LHX] .

PINS FSB-CTLIN+ FSB-CLKIN+ FSB-CADIN+

PINS FSB-CTLOUT+ FSB-CLKOUT+ FSB-CADOUT+
```



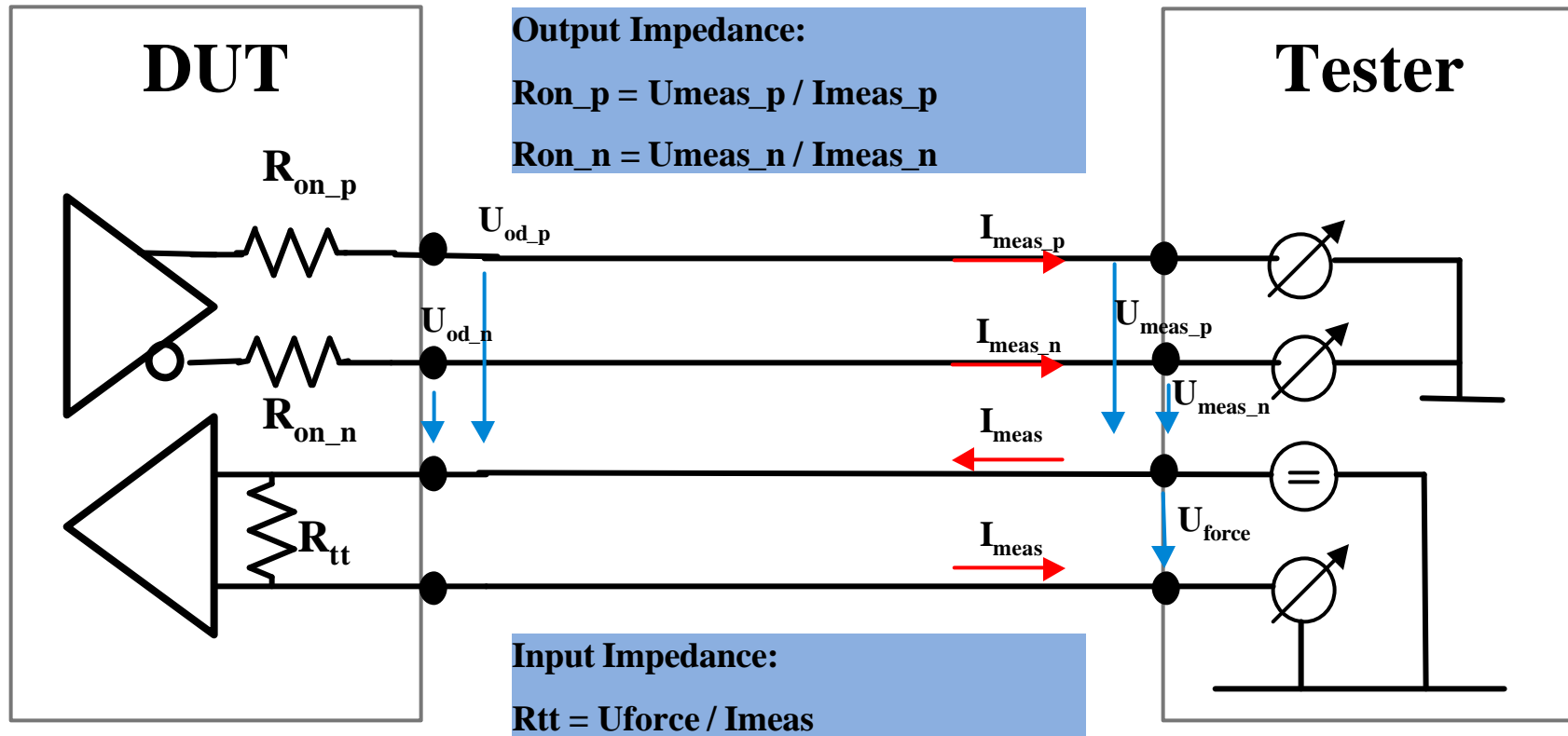
Application Example: SONET Chip (OC48)



Test List for High-Speed Interfaces

<i>TEST LIST</i>	<i>ATE NEEDS</i>
Impedance Test (Input, Output)	DC Access
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability
Receiver Skew Insertion	Timing Accuracy & Resolution
Transmitter Skew Measurements	Timing Accuracy, High Linearity
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth
Rise/Fall Time Measurements.	High Bandwidth, High Resolution
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy
Jitter Test	Low System Jitter, All Others
Source Synchronous Test	Source Synchronous Mode
HV Production Solution	Full Integrated Solution, High Throughput

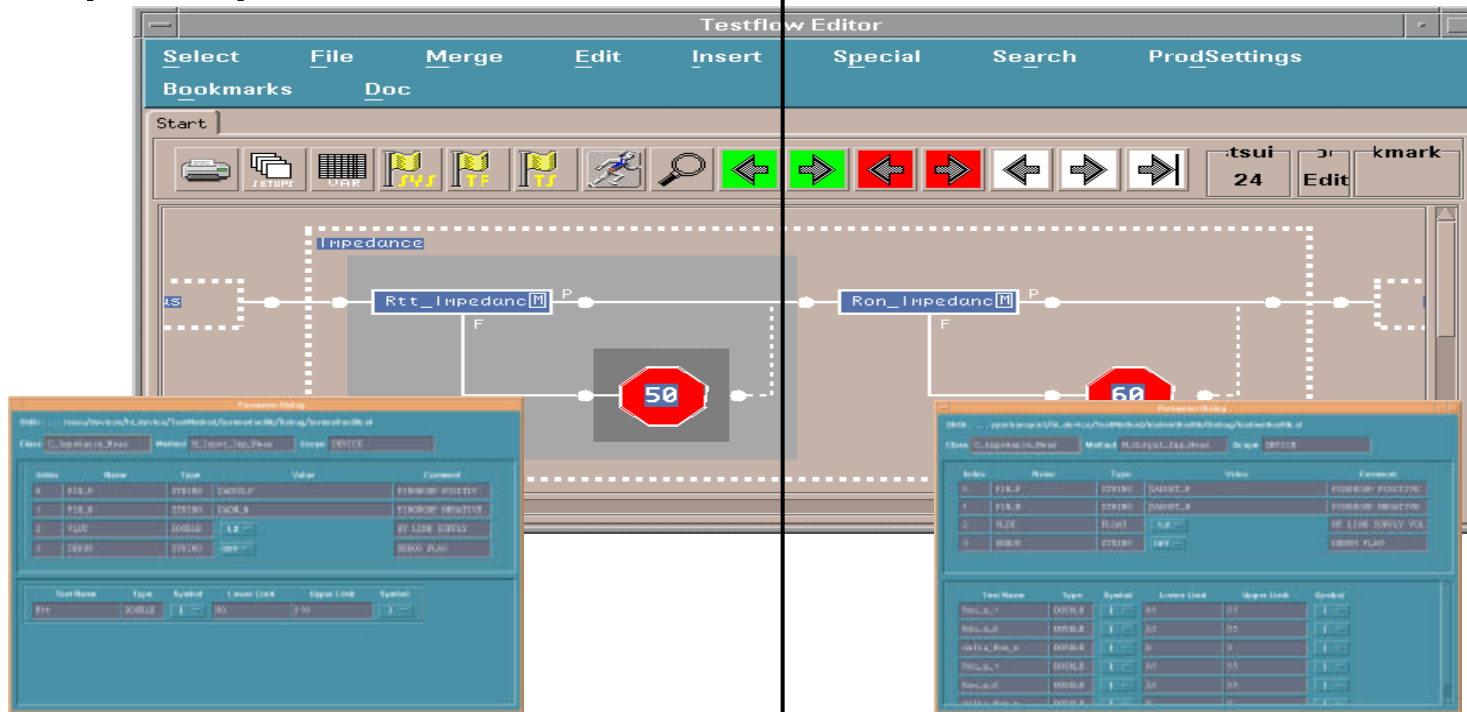
Impedance Test: Theory



Impedance Test: Tester Setup

- Input Impedance

- Output Impedance



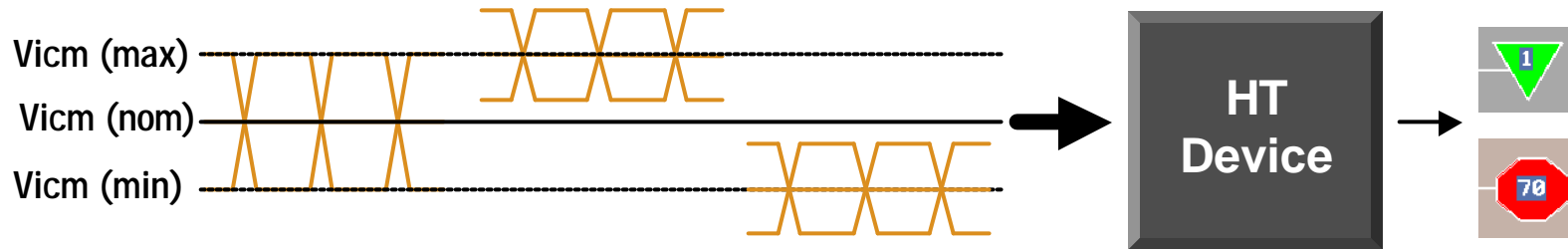
- Pre-condition your device
- Force voltage: U_{force}
- Current measurement: I_{meas}
- Calculate Input Impedance: $R = U_{force} / I_{meas}$
- Pass/Fail decision

- Pre-condition your device
- DVM measurement: U_{meas}
- Current measurement: I_{meas}
- Calculate Input Impedance: $R = U_{meas} / I_{meas}$
- Pass/Fail decision



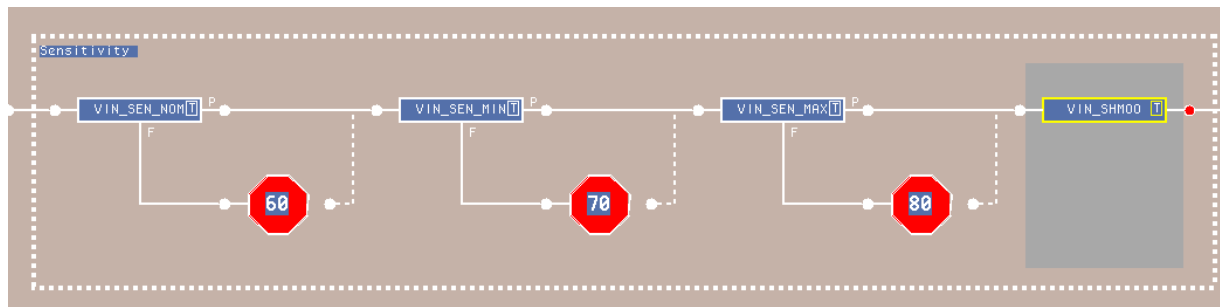
At Speed Receiver Test: Sensitivity Test

Input Sensitivity Test:



- For RX functional test, different level sets can be used to run at the specified limits
- Requires only one functional pattern to test the part to its limits

Tester Setup:



```
#####
# Equation Set for Level Sensitivity Test:
# Level Set 1:VLDT_NOM = 1.20V  VID_NOM = 600mV  VICM_NOM = 600mV
# Level Set 2:VLDT_MIN = 1.14V  VID_MIN = 200mV  VICM_MIN = 440mV
# Level Set 3:VLDT_MAX = 1.26V  VID_MAX = 1000mV  VICM_MAX = 780mV
#####
EQNSSET 2 "diff_level_eqn"

MODECONTEXT "differential"

SPECS
VLDT [V] # HyperTransport Link Supply Voltage
VID [V] # Input differential voltage
VICM [V] # Input common-mode voltage
I_LIMIT [mA]

EQUATIONS
VIH = VICM + VID/2
VIL = VICM - VID/2

DSPINS VTI
vout = VLDT
defcort = act
ilimit = I_LIMIT
t_ms = 5

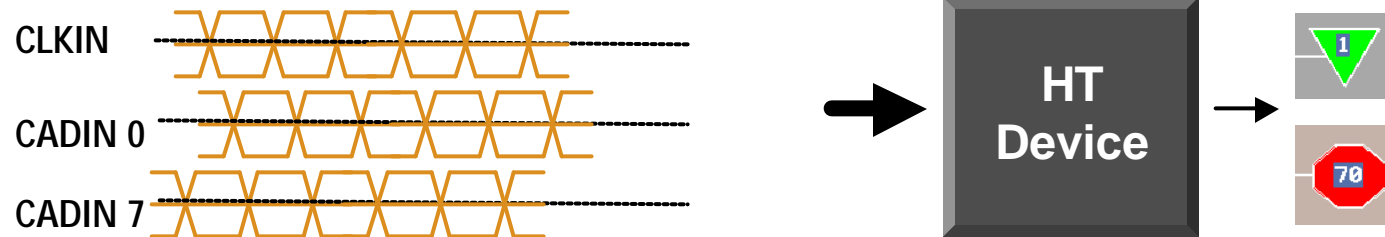
LEVELSET 1 "diff_tap_lset"

PINS CADIN_N CADIN_P
v1l = VIL
v1h = VIH

PINS CLKIN
v1l = VIL
v1h = VIH
```

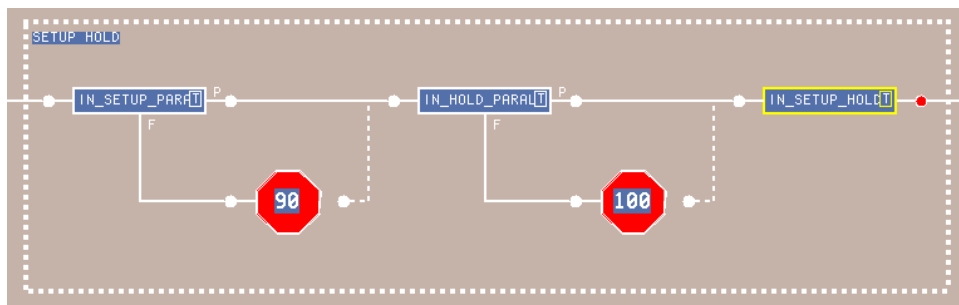
At Speed Receiver Test: Skew Insertion

Input InterSkew Test:



- Program skew for all pins independently with spec variable
- Requires only one functional pattern to test the part to its limits

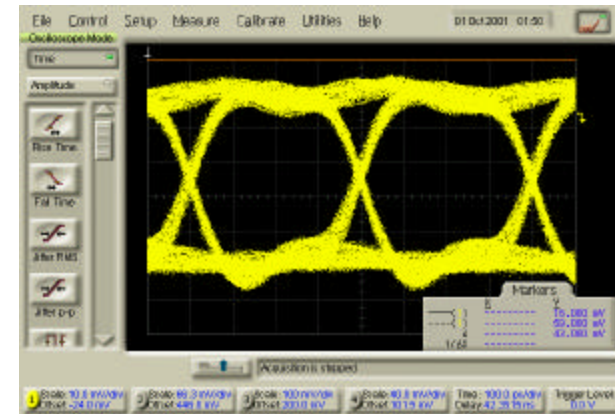
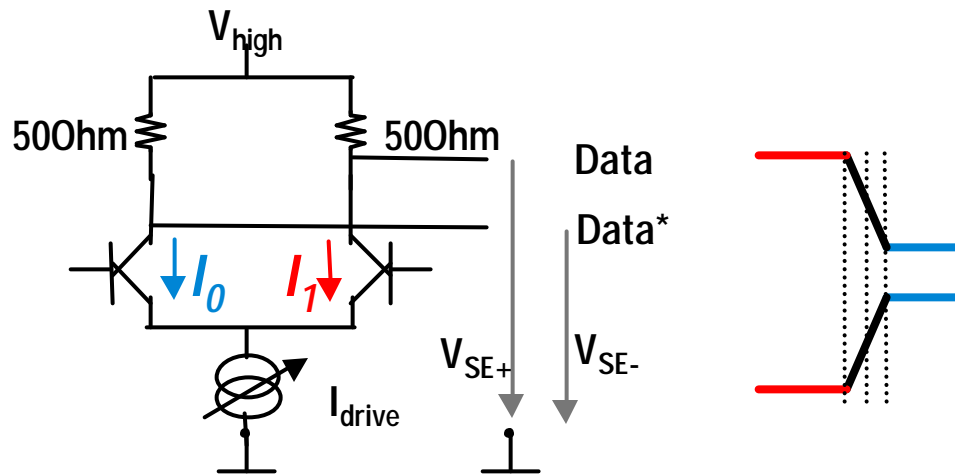
Tester Setup:



Test Control		
Edit Doc		
Functional Test		
Parametric		
[run to]	vector	
[mask before]	cycle	
[mask after]	cycle	
[result pins]	parallel	out_pins
[spec name]	timing	t_setup_off
[setup pins]	parallel	CADIN
[method]	serial	
[start]	ns	0
[stop]	ps	#(@Tbit%T/2)
[step]	ps	#20
[resolution]	ps	0.01
[pass min]	ps	0
[pass max]	ps	116
output	PFunc (\$P)	

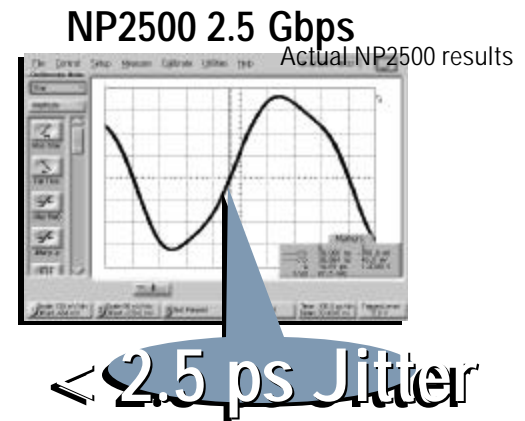
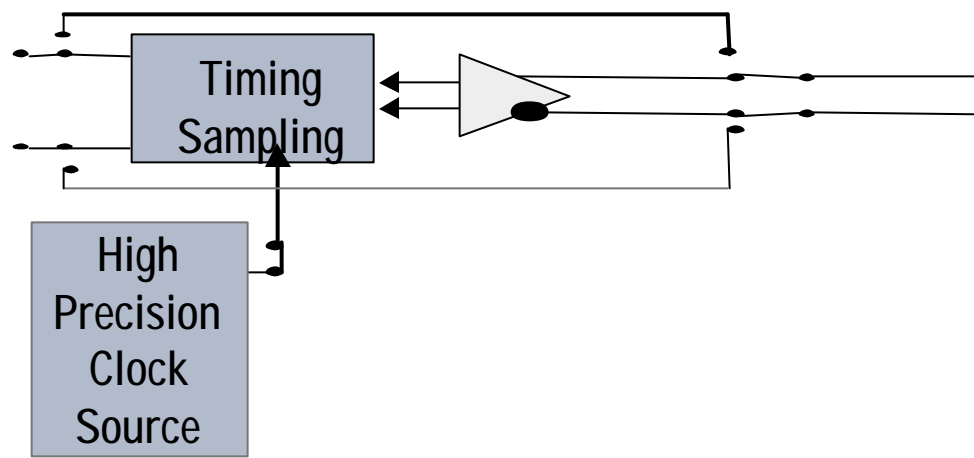
NP-Model Native Differential Driver

Differential Driver: Current Switch



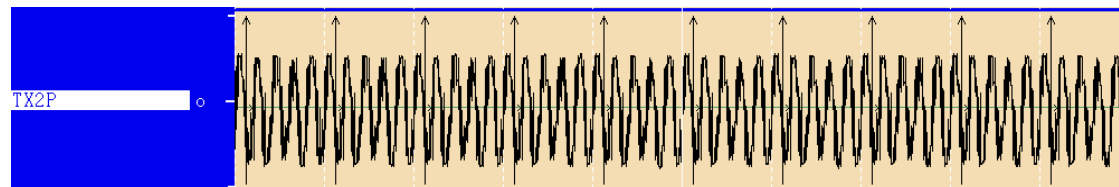
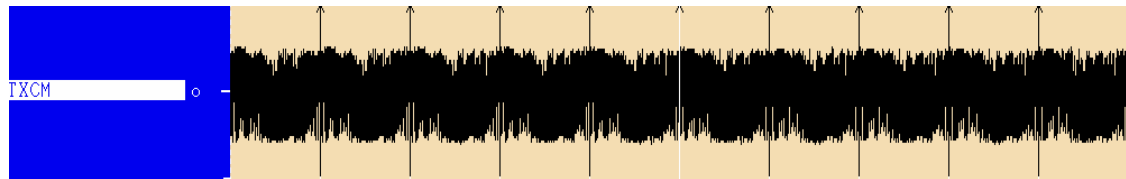
PRBS: 2.5 Gbps, 50 mV Swing

Retiming Unit:



Fast Debug with Timing Diagram

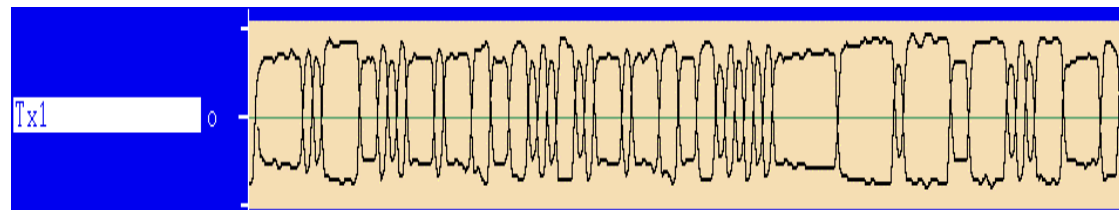
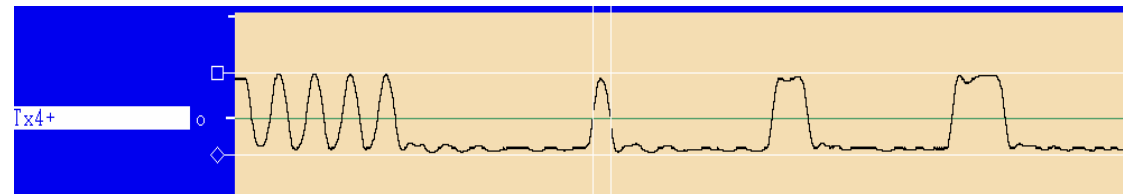
- PLL is not locked



- Device Jitter

- Level verification

- Timing verification



- Crossover Symmetry

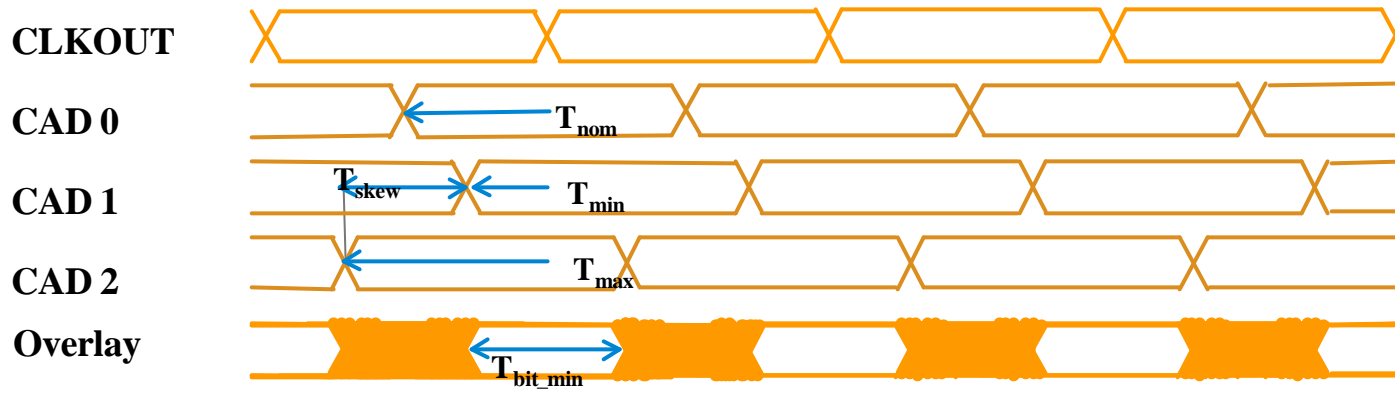
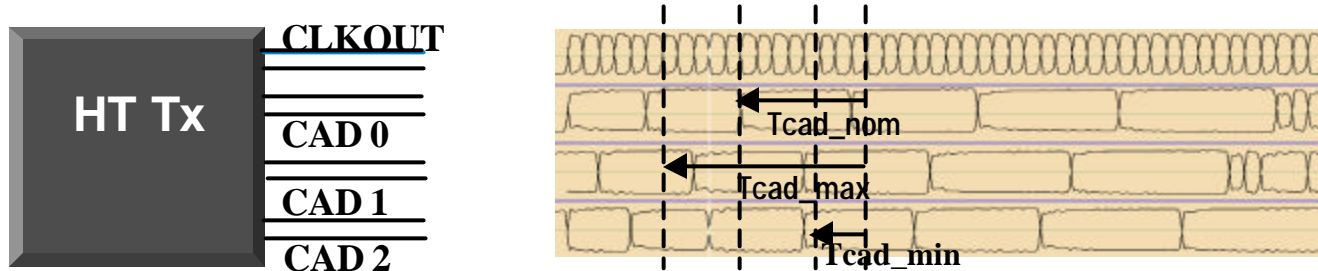
- Pattern verification

- Common mode shift, Cross Talk, and many more

Fast Visual Feedback-Over a Wide Range!

Clock-Data Output Skew: Theory

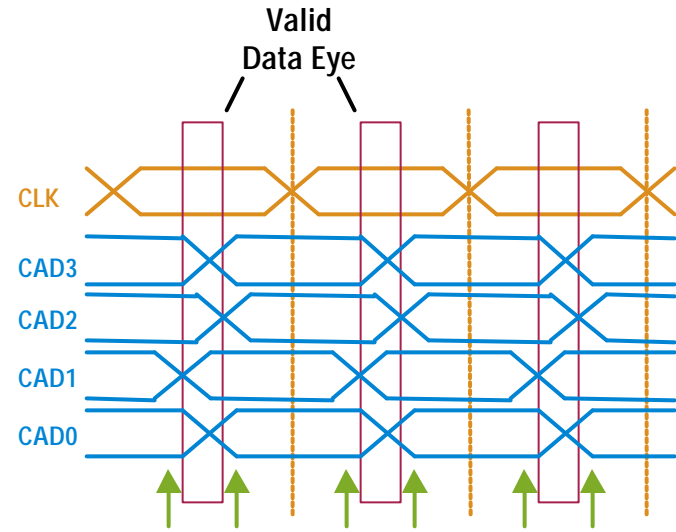
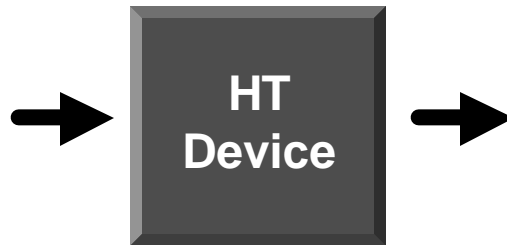
Device
Output:



- T_{nom} = Nominal setup time between Clock and Data/Control
- T_{min} = Minimal setup time
- T_{max} = Maximal setup time
- T_{skew} = Maximal skew between data line $T_{max} - T_{min}$

At Speed Transmitter Test: Functional

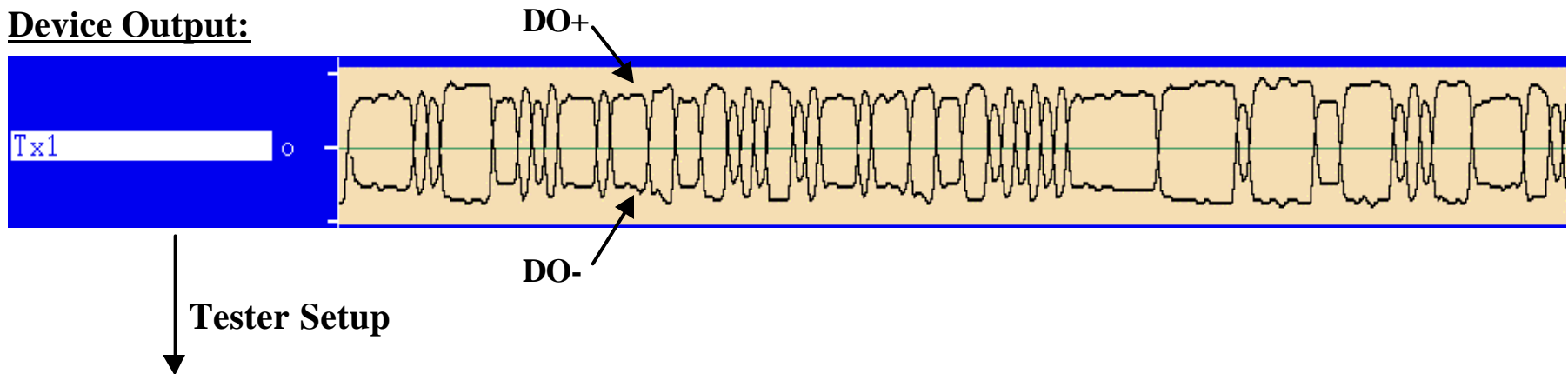
Pin/ Group Names	P o u t P o l	F x l o c k d e t i	t s d n l	t s d p l
pin mask DD/ED/name format	DevCyc	DevCyc	DevCyc	DevCyc
12766	XXX	XXX	LLLLHHHHH	HHHLLLLLL
12767	XX	XX	LHHHHLLH	HLHLLHLL
12768	XXX	XXX	HHLHLLHLL	LLHLLHLLH
12769	XX	XX	LLHLLHLLH	HLHLLHLLH
12770	XXX	XXX	LHLLHLLH	HLHLLHLLH
12771	XX	XX	LHLLHLLH	HLHLLHLLH
12772	XXX	XXX	HHHLLHLLH	LLHLLHLLH
12773	XX	XX	LHLLHLLH	HLHLLHLLH
12774	XXX	XXX	LHLLHLLH	HLHLLHLLH
12775	XX	XX	LHLLHLLH	HLHLLHLLH
12776	XXX	XXX	LHLLHLLH	HLHLLHLLH
12777	XX	XX	LLHLLHLLH	HLHLLHLLH



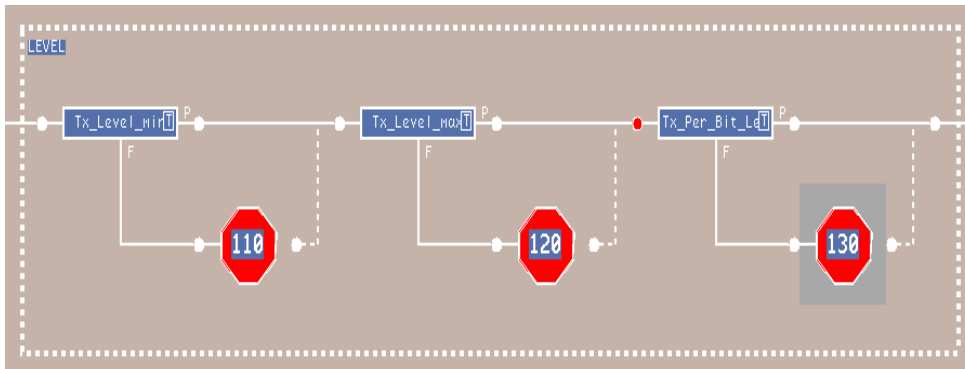
- Search the clock edge (Tclk) and
- Program relative to the Tclk the edge delays
- $T_{\text{valid}} = T_{\text{bit}} - 2 * T_{\text{cad_min}}$
- Apply a large pattern to guaranty worst-case output skew.

At Speed Transmitter Test: Voltage

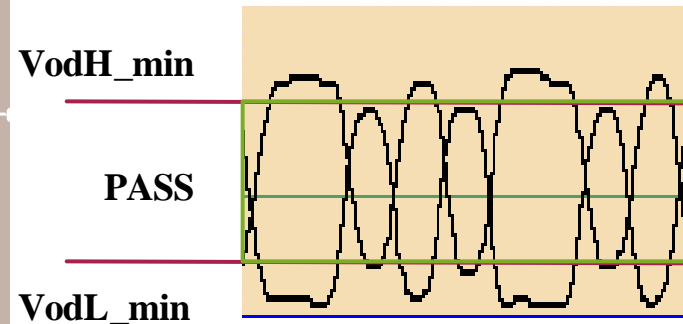
Device Output:



Testflow:

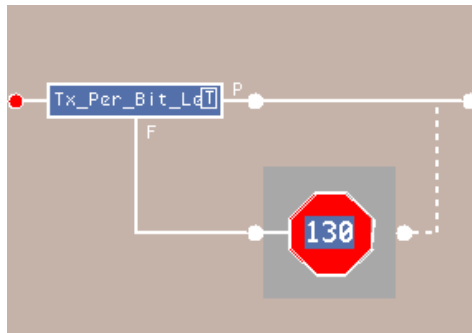
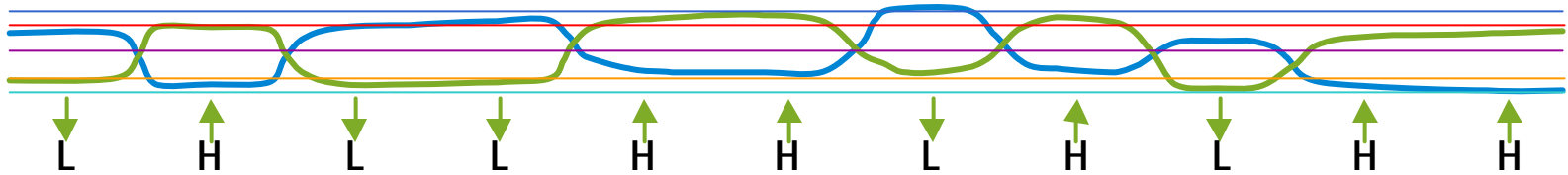


Minimum Output Voltage:



- Measure over a large number of samples to measure worst-case output voltage.

Per Bit Voltage Measurement



Overlay of N and P Out

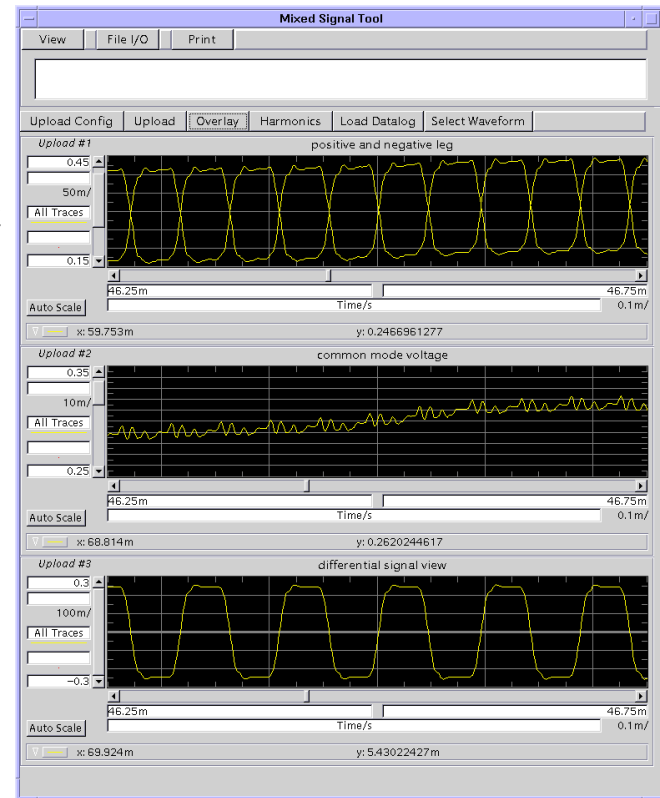
Parameter Dialog

Index	Name	Type	Value	Comment
0	Bit	STRING	0110101	Pre-Fixator 01 100
1	StartBit	INT	0	Start bit to be 28
2	StopBit	INT	30000	Last bit to be 700
3	ElectroMag	STRING	DepDelay	Change spec 742106

Test Name	Type	Option	Lower Limit	Upper Limit	Symbol
DIFF - swing	DIFFER		0.4	0.6	
CM - voltage (Vcm)	DIFFER		0.2	0.30	
CM - variation	DIFFER		0	0.5-0.5	

Output Vcom

Output Vswing

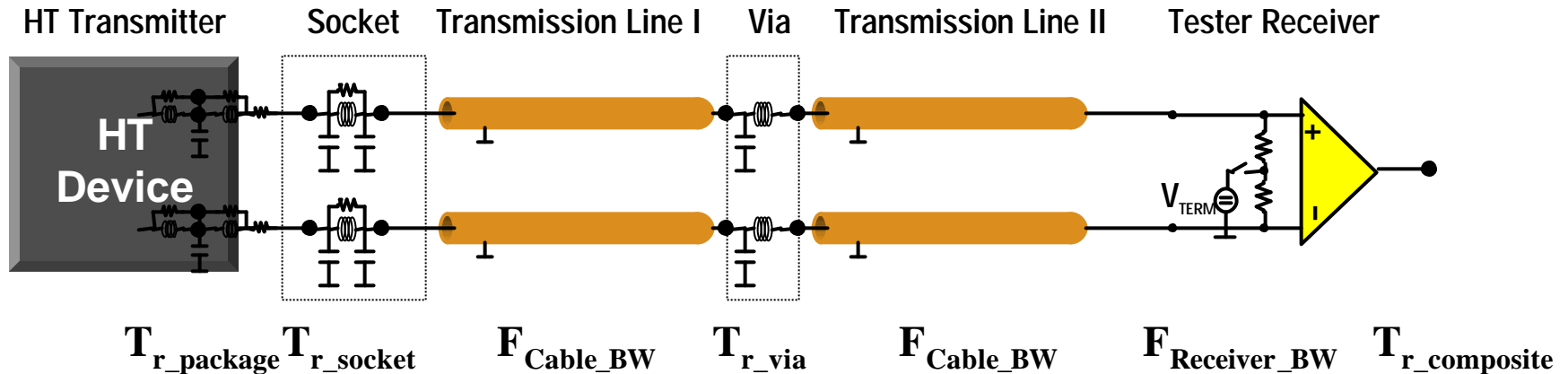


Summary

<i>TEST LIST</i>	<i>ATE NEEDS</i>	<i>COVERED</i>
Impedance Test (Input, Output)	DC Access	✓
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability	✓
Receiver Skew Insertion	Timing Accuracy & Resolution	✓
Transmitter Skew Measurements	Timing Accuracy, High Linearity	✓
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth	✓
Rise/Fall Time Measurements.	High Bandwidth, Resolution, Low Overdrive	
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy	
Jitter Test	Low System Jitter, All Others	
Source Synchronous Test	Source Synchronous Mode	
HV Production Solution	Full Integrated Solution, High Throughput	✓

Rise/Fall Time Measurements: Theory

Transmission Path:



$$T_{composite} = \sqrt{T_{r_device}^2 + T_{r_package}^2 + T_{r_socket}^2 + T_{r_via}^2 + T_{r_cable}^2 + T_{r_BW}^2}$$

DUT Board considerations:

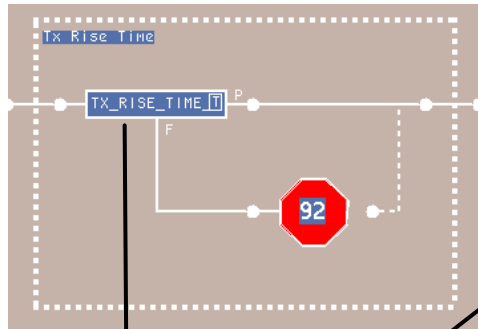
- Uniform trace impedance across the whole trace (reflections)
- Vias and other potential impedance discontinuities should be minimized (reflections)
- Make your trace width as wide as possible (skin effect)
- Talk to your PCB manufacturer about modeling techniques used

More Details:

- Hall, Hall, McCall: "High-Speed Digital System Design"
- Johnson, Graham: "High-Speed Digital Design"

Rise/Fall Time Measurements: Setup

Testflow:



```
PINS tsdp1
# USED WAVEFORMS 0 1 2 3 4 5 6 7 8 9 a b c d e f 10
15 16 17 18 19 1a 1b 1c 1d 1e 1f
r1=time_ps*transmit_output_strobe + Tx1_offset #RU
```

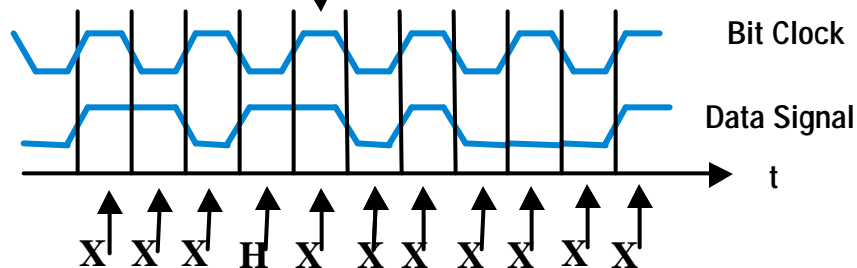
```
PINS tsdp1 tsdn1
term scope+
vt = CML_swing/2
vth = V_TRESHOLD
```

	X-axis	Y-axis
specname	transmit_output_	V_TRESHOLD
type	timing	level
[s_pins]	tsdp1	
[unit]	ps	V
start	350	-0.08
stop	450	0.42
step	#100	#100

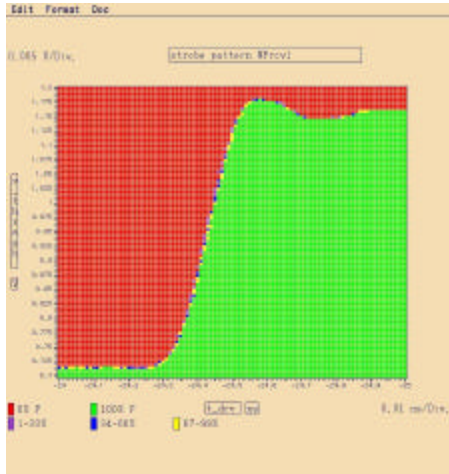
[result pins]

[test filename]

[test mode]

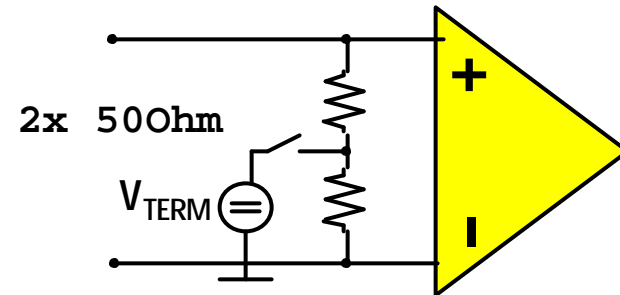


Rise/Fall Time Measurements: Results



120 ps Rise Time
@400 mV Swing
@ the Receiver!

Differential Comparator



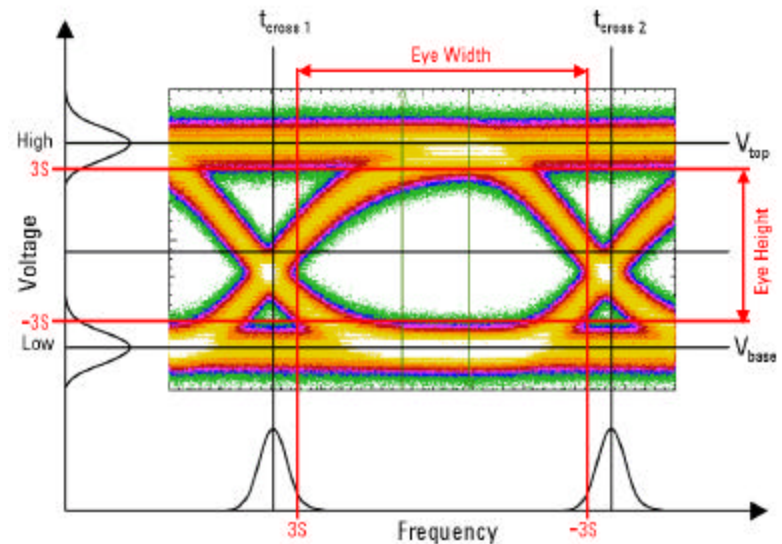
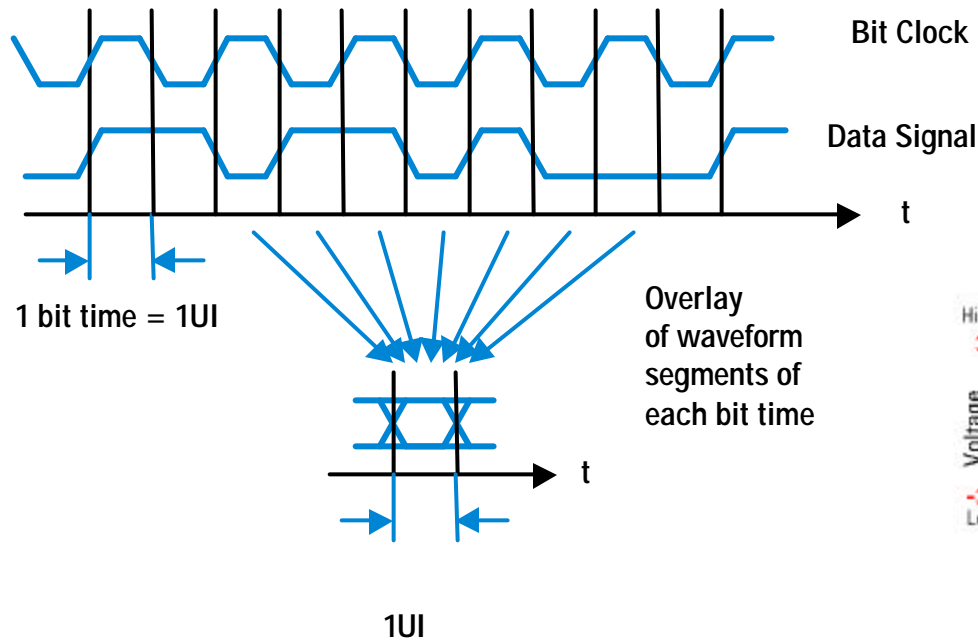
The Receiver matches the Application

- True differential
- Floating (and center tap) termination
- Outstanding bandwidth
- Built-in scope capability up to 2.5 Gbps

Debug and Test the REAL DUT output!

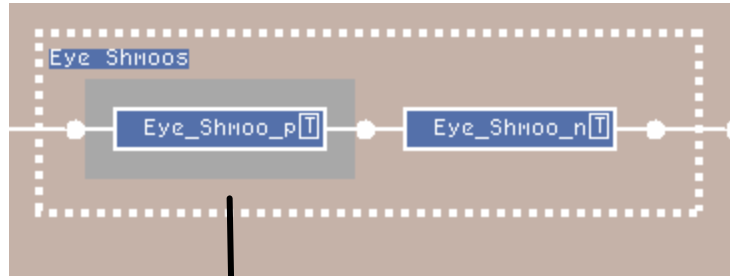
Eye Diagram: Theory

Eye diagram is an overlay of many waveforms recorded with a bit clock as a trigger. This is an important parametric characteristics of the high speed transmit interface. Rise time/Fall time, jitter, and signal levels, overshoot, undershoot, ripple can be extracted from an eye diagram.

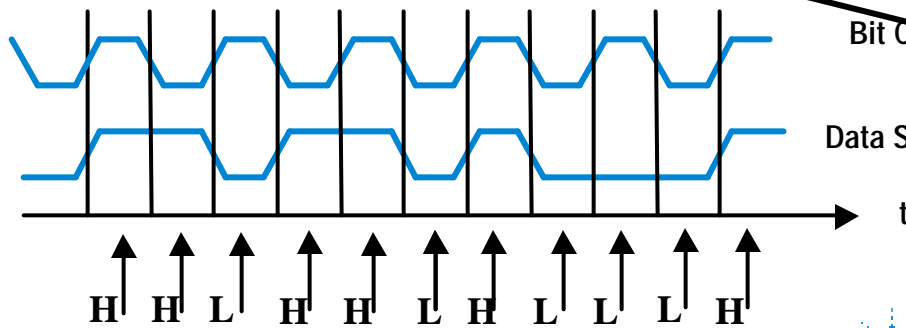
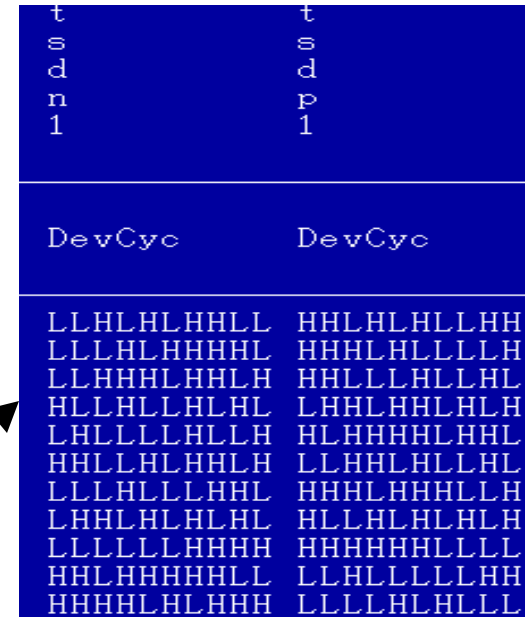


Eye Diagram: Setup

Testflow:



The screenshot shows the configuration window for 'Eye_Shmoos_p'. It includes fields for 'Testsuite name', 'Timing Equation', 'Timing Spec Set', 'Timing Set', 'Level Equation', 'Level Spec', 'Level Set', 'Analog Set', 'Vector Label', 'Context', and 'Testfunction'. A 'Testfunction' tab is selected. On the right, there are buttons for 'Load', 'Select', 'Edit', 'Modify TestMethod', 'New Testfunction', 'Exec All & Stop Here', 'Execute', 'Cancel', and 'Done'.



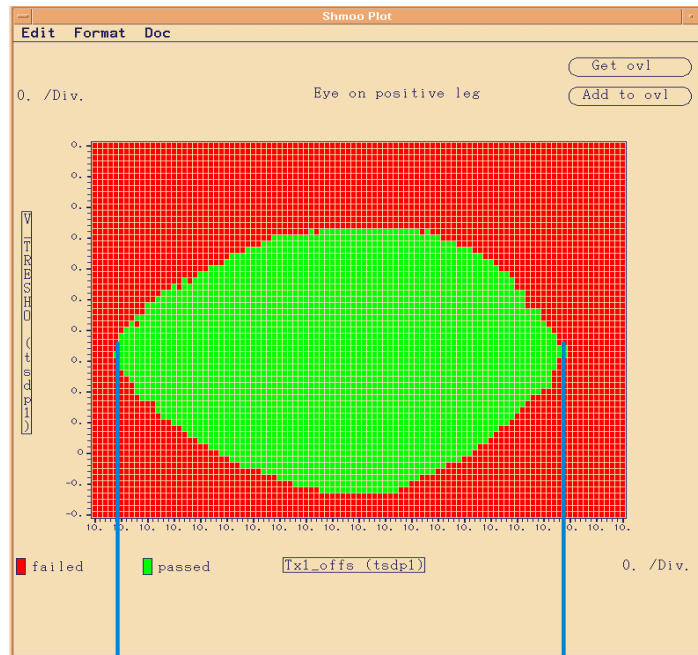
The screenshot shows the 'Test Control' window with the 'Shmoos Spec' configuration. It includes a title field 'Eye Diagram P', a table for 'specname', 'type', '[s_pins]', '[unit]', 'start', 'stop', and 'step'. Below the table are fields for '[result pins]', '[test filename]', and '[test mode]'.

specname	X-axis	Y-axis
Tx1_offset@other		V_TRESHOLD
type	timing	level
[s_pins]	tsdpl	tsdpl
[unit]		
start	-200	-0.1
stop	200	0.5
step	#100	#100

[result pins] tsdpl
 [test filename]
 [test mode] normal

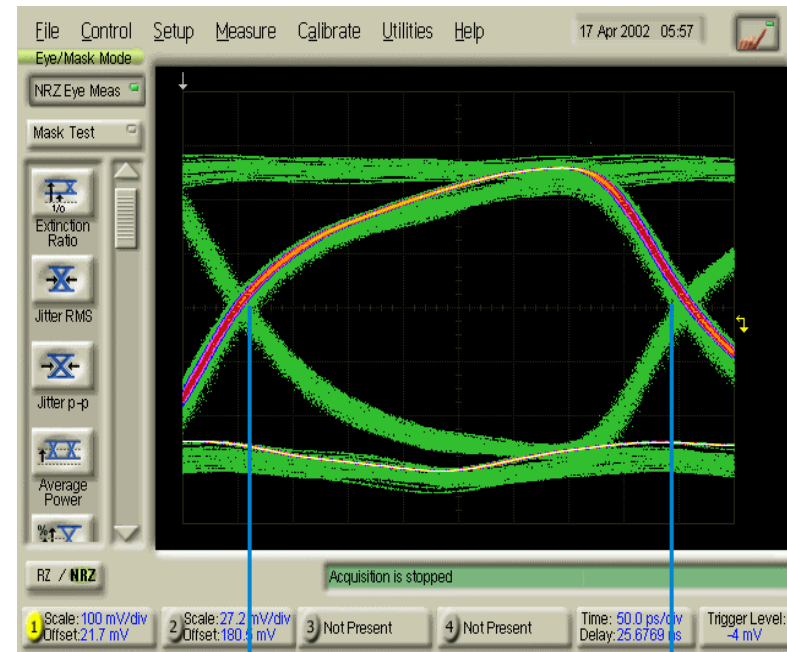
Eye Diagram: Results I

Real Device Out @ 2.5 Gbps: Eye Shmoo:



← 352ps →

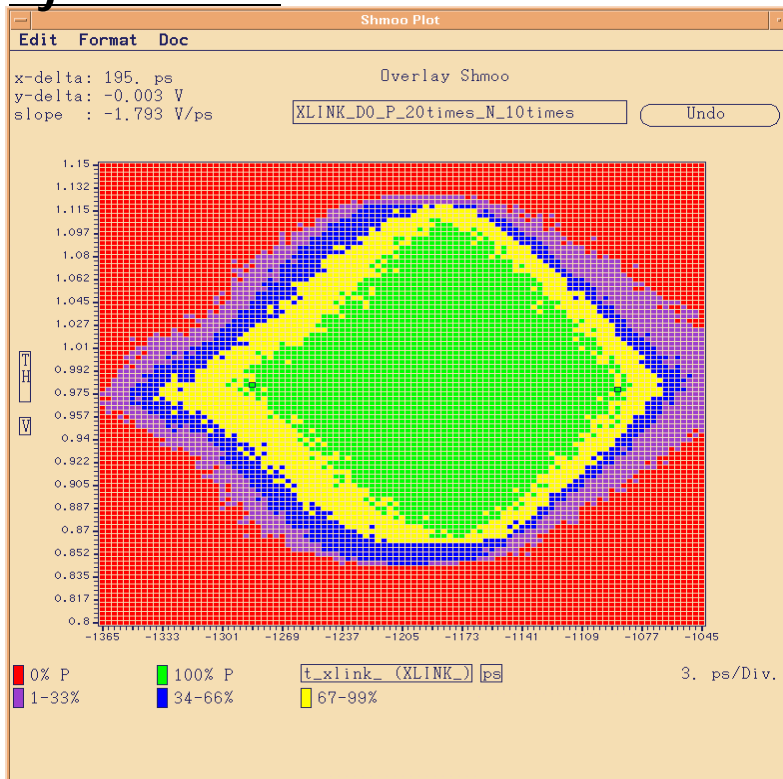
DCA:



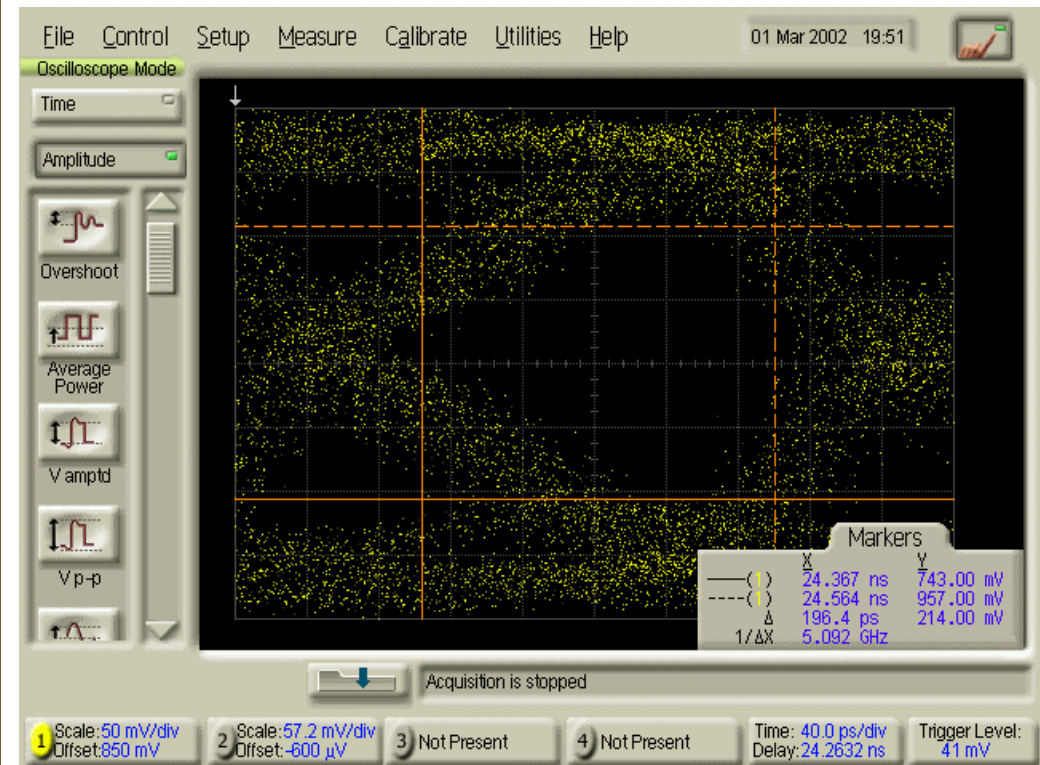
← 350.5ps →

Eye Diagram: Results II

Real Device Out @ 3.125 Gbps:
Eye Shmoo:



DCA:



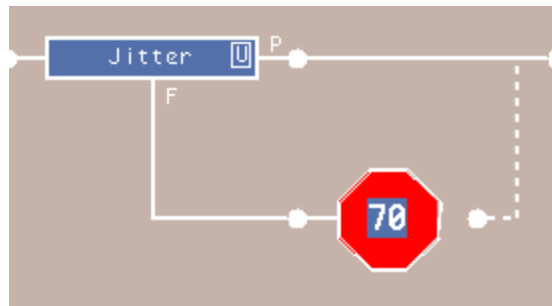
See the REAL DUT output!

Jitter Measurements

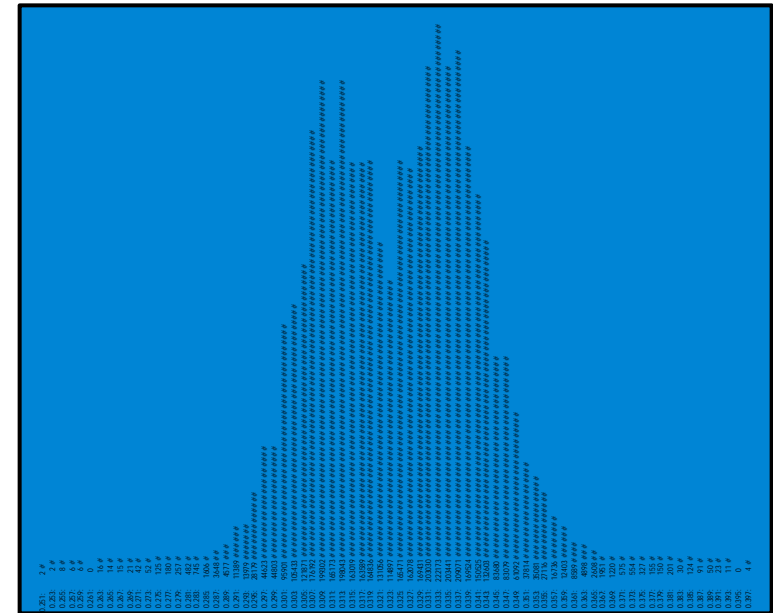
1) Apply PRBS Pattern

Pin/Group Names	P o u t P O I	r x l o c k d e t i	t s d n l	t s d p l
pin mask DD/ED/name format	DevCyc	DevCyc	DevCyc	DevCyc
12766	XXX	XXX	LLLLHHHHH	HHLLLLLLL
12767	XX	XX	LHHHHLLHH	HLLLLHLLL
12768	XXX	XXX	HHLHLLHHH	LLHLLHHH
12769	XX	XX	LLHLLHHLL	HLLHLLHLL
12770	XXX	XXX	LLHLLHLLH	HLLHLLHLL
12771	XX	XX	LHLLHLLHL	HLHLLHLLH
12772	XXX	XXX	HHLHLLHHH	LLHLLHHH
12773	XX	XX	LHLLHLLHL	HLHLLHLLH
12774	XXX	XXX	LHLLHLLHL	HLHLLHLLH
12775	XX	XX	LHLLHLLHL	HLHLLHLLH
12776	XXX	XXX	LHLLHLLHL	HLHLLHLLH
12777	XX	XX	LLHLLHLLH	HLLHLLHLL

2) Measurements & Calculation



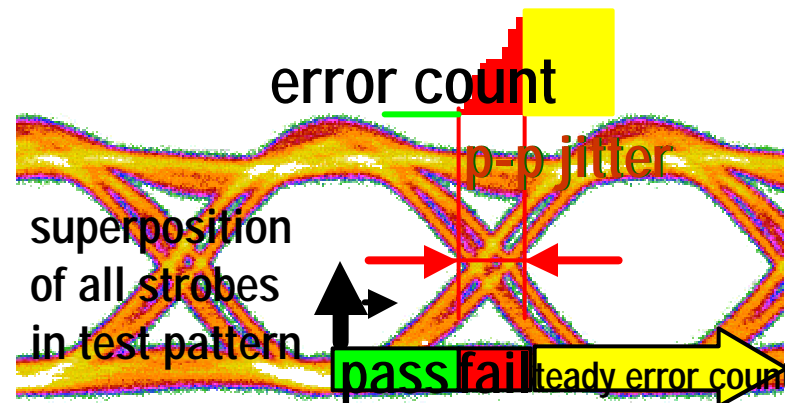
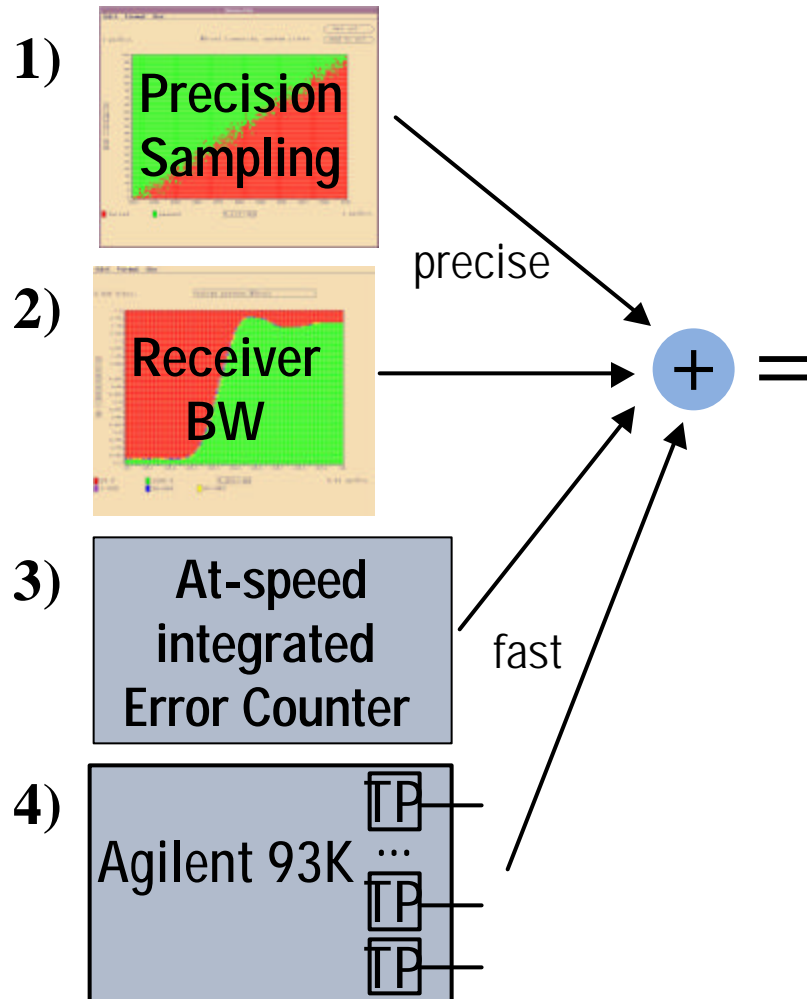
3) Histogram



- Jitter Test at full speed on a PRBS Pattern
- Returns PP & RMS Value, etc.
- Real-time compare without capture & upload
- No additional instrument needed

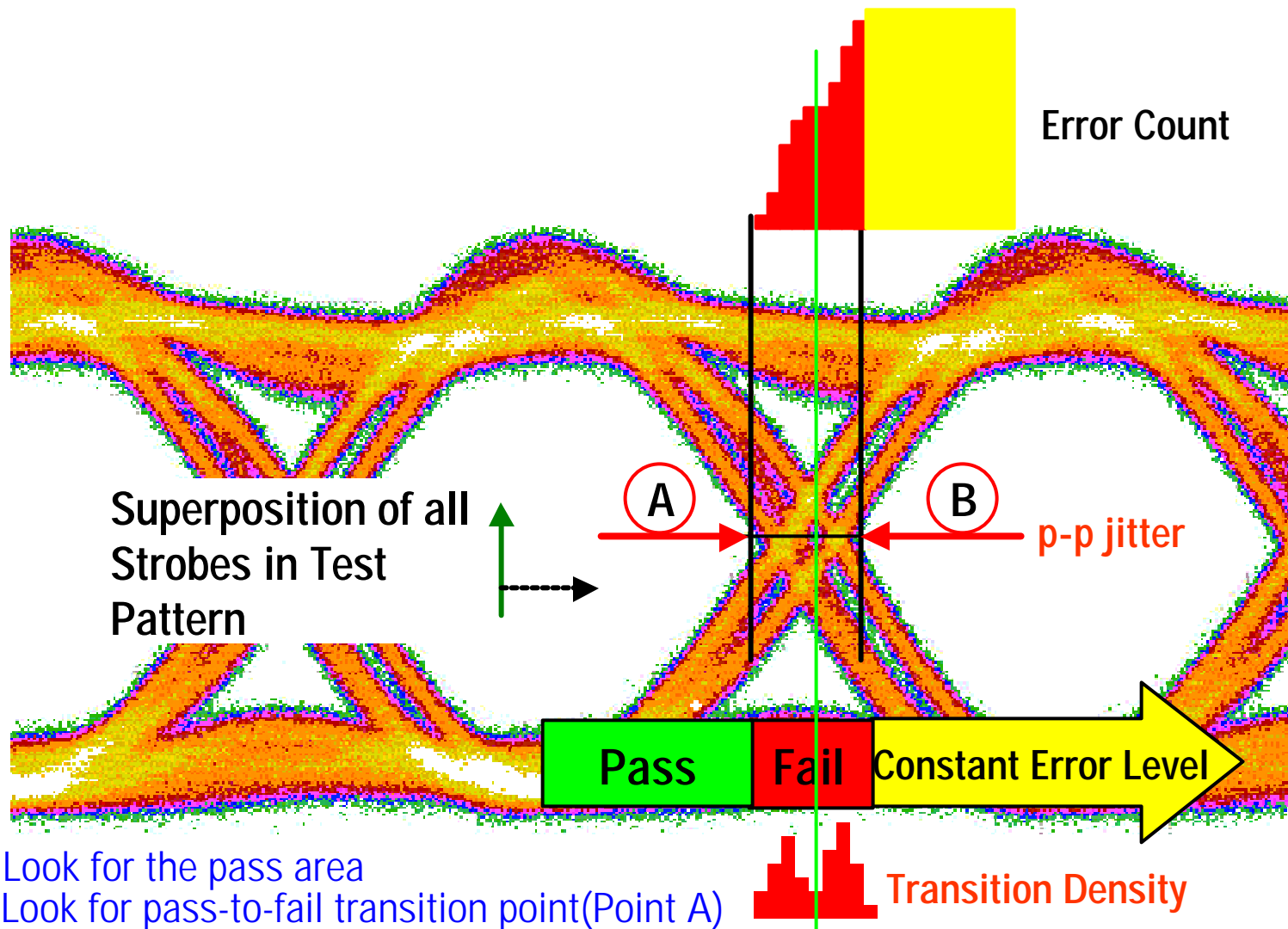
Identify Your Device Jitter FAST!

Ultra Fast Jitter Measurements



- Highly linear timing delay circuits per pin (5ps)
- Resolution down to 1 ps
- Superior comparator bandwidth
- Test Processor-Per-Pin Architecture for PARALLEL execution
- Error Counter

Jitter Measurement: Theory



1. Look for the pass area
2. Look for pass-to-fail transition point(Point A)
3. Use 93K Error Count feature to look for max error count, take it as Point B
4. The time difference between Point A & Point B is considered as peak-to-peak jitter

Implementation

The screenshot shows a testbench sequence with the following steps and statistics:

- START**: nmb: 1, ave: 6.203ms
- hoadjust_funcT**: nmb: 1, ave: 817.630ms
- SyncTxMeasJitU**: nmb: 1, ave: 2.233ms
- func_after_syT**: nmb: 1, ave: 2.233ms

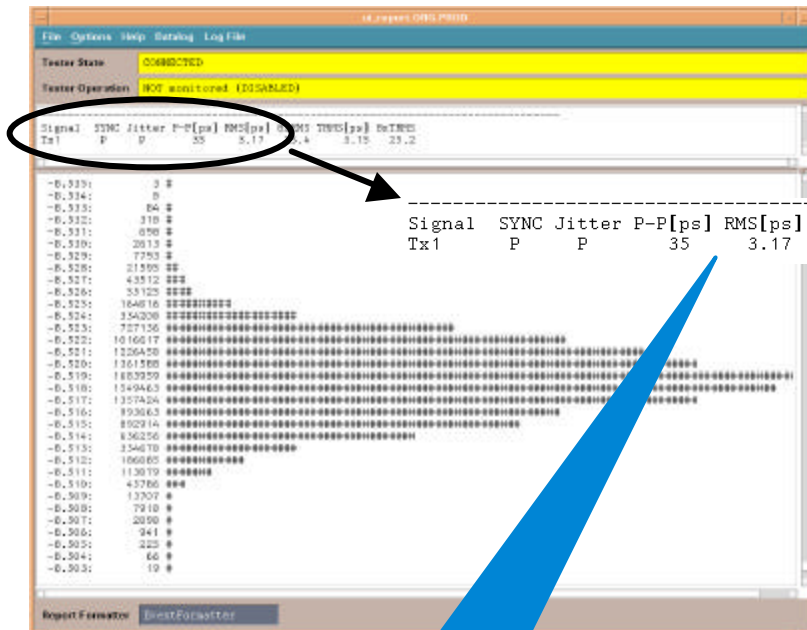
The **SyncTxMeasJitter** configuration window is shown with the following details:

- Testfunction**: (unselected)
- Testmethod**: (unselected)
- Userprocedure**: (selected)
- Testsuite name**: SyncTxMeasJitter
- Userproc name**: SyncTx 0 63 4 3 -16 40 0.2
- Timing Equation**: 1, standard
- Timing Spec Set**: 1, 250 Mbps
- Timing Set**: 1, standard
- Level Equation**: 1, standard
- Level Spec**: 1, 3V
- Level Set**: 1, single threshold
- Analog Set**: (empty)
- Vector Label**: "jitter_pattern"

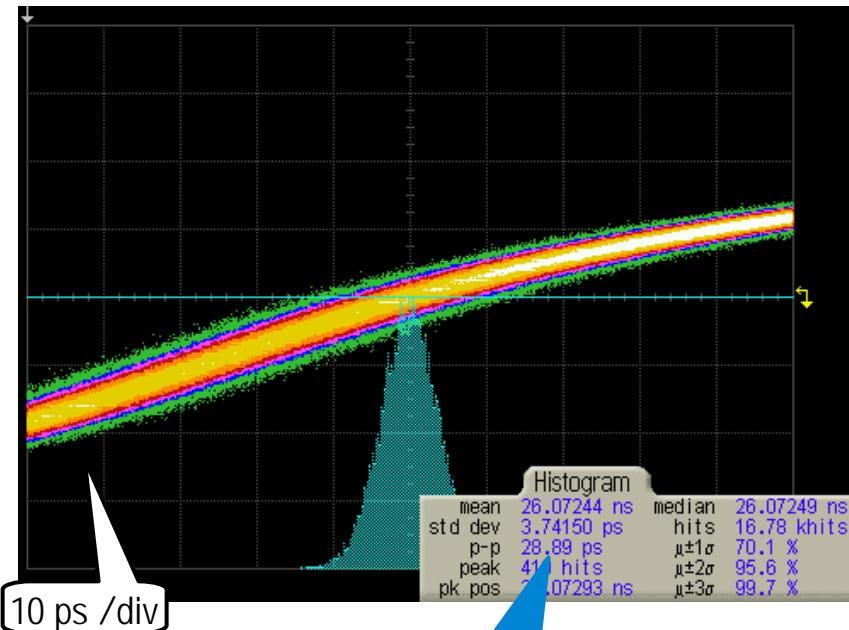
Input for Userproc. (examples only):

- 0 = min. pin
- 63 = max. pin
- 4 = bit time - period (ns)
- 3 = min_open_eye (ns)
- 16 = start offset (ns)
- 40 = stop offset (ns)
- 0.2 = pass_max_jitter (ns)

Measurement Results: SerDes Device with Clock Signal

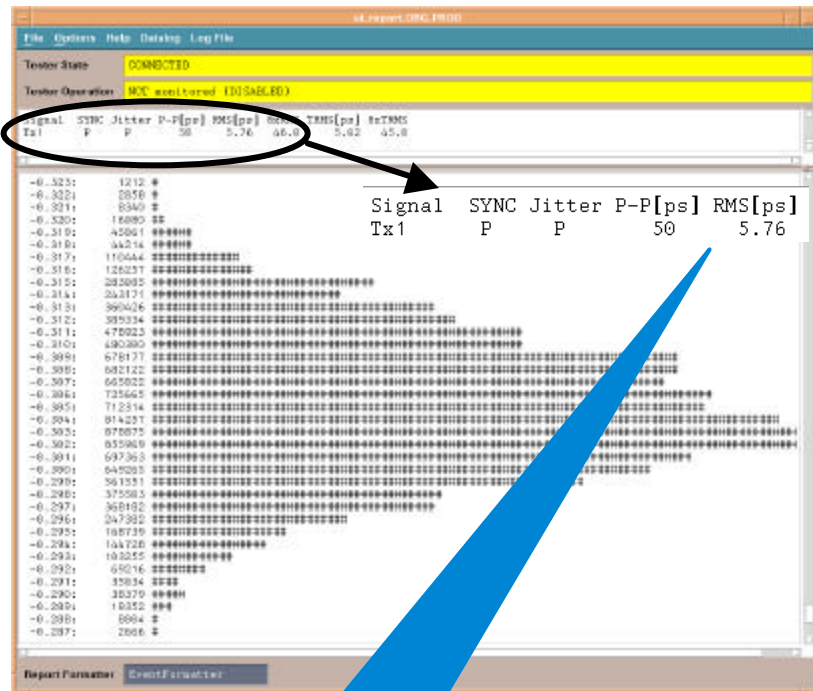


Random Jitter
35 ps p-p
3.57 ps RMS

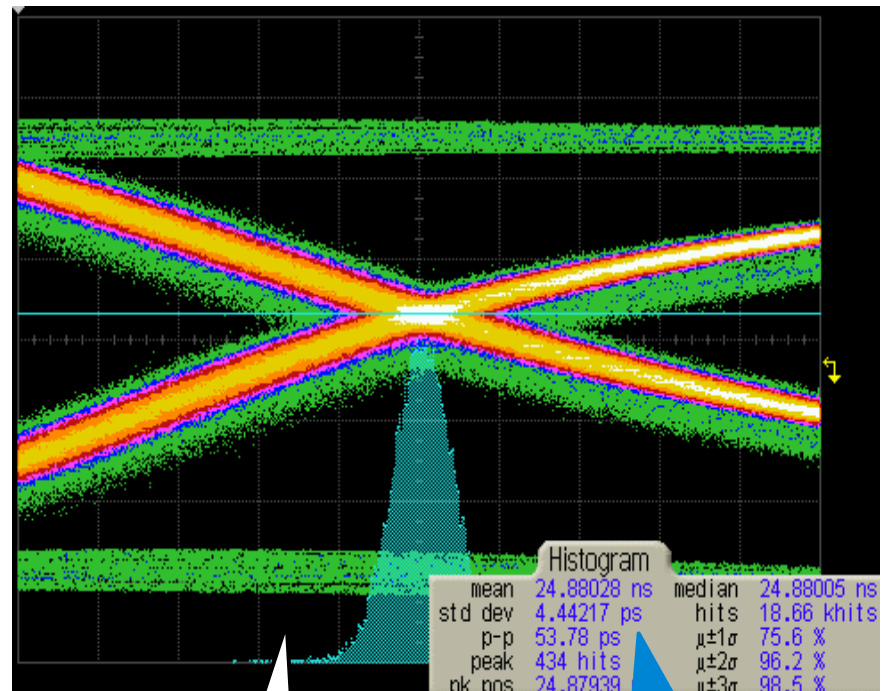


Random Jitter:
28.9 ps p-p
3.74 ps RMS

Measurement Results: SerDes Device with Data Pattern (DDJ + RJ)



50 ps p-p Jitter!

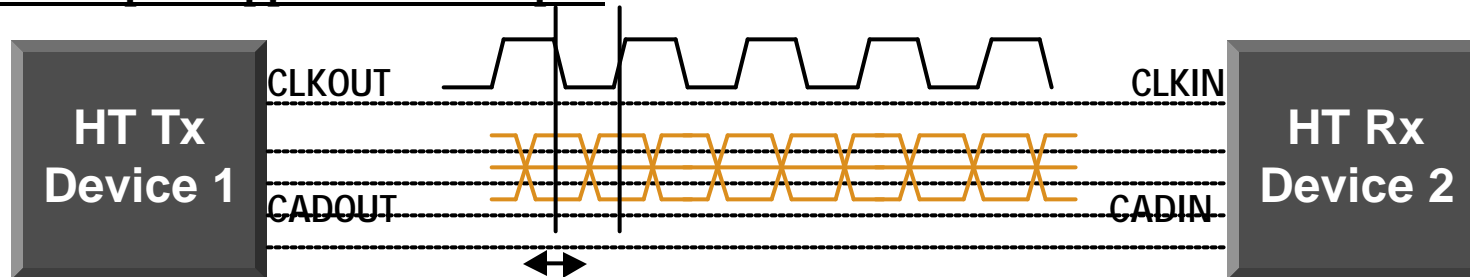


10 ps / div

53.8 ps p-p Jitter!

The Source Synchronous Test Challenge

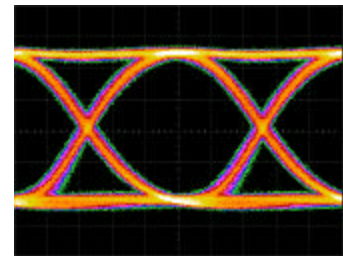
HyperTransport Application example:



- CLKOUT shows Accumulated Phase Shift of PLL.
- CADOUT moves with phase shift.

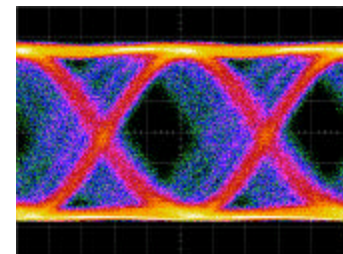
• What does the HT receiver see?

- Sampling Clock moves with shift
- Data eye stays open

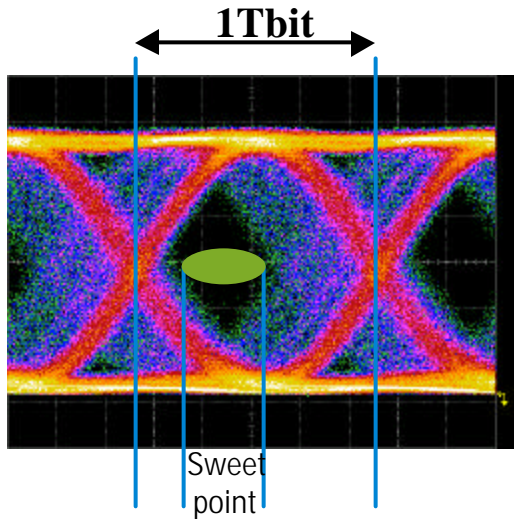


• What does a "standard" ATE see?

- Sampling Clock is fixed
- Data eye closes



None Source Synchronous Tester



- What is the minimum EPA a tester needs?

$$t_{\pm EPA} \leq \frac{\Delta t_{Bit} - \Delta t_{CumPhasErr} - \Delta t_{ProcessMargin}}{4}$$

- Calculation example with:

- 1) 1UI = 800 Mbit Tbit = 1.25 ns
- 2) 1UI = 1.6 Gbit Tbit = 625 ps
& Cum Phase Error = +/-250ps
& Process Variation = +/- 50ps

$$1) \quad t_{\pm EPA_800\ Mbit} \leq \frac{1.25\ ns - 500\ ps - 100\ ps}{4} = 162.5\ ps$$

$$2) \quad t_{\pm EPA_1.6\ Gbit} \leq \frac{625\ ps - 500\ ps - 100\ ps}{4} = 6.25\ ps$$

Conclusion:

- Beyond the Gigabit you will need a tester which operates Source Synchronous

Summary

<i>TEST LIST</i>	<i>ATE NEEDS</i>	<i>COVERED</i>
Impedance Test (Input, Output)	DC Access	✓
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability	✓
Receiver Skew Insertion	Timing Accuracy & Resolution	✓
Transmitter Skew Measurements	Timing Accuracy, High Linearity	✓
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth	✓
Rise/Fall Time Measurements.	High Bandwidth, Resolution, Low Overdrive	✓
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy	✓
Jitter Test	Low System Jitter, All Others	✓
Source Synchronous Test	Source Synchronous Mode	✓
HV Production Solution	Full Integrated Solution, High Throughput	✓

