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Testing High-Speed HyperTransport Interfaces on Agilent 93000 SOC

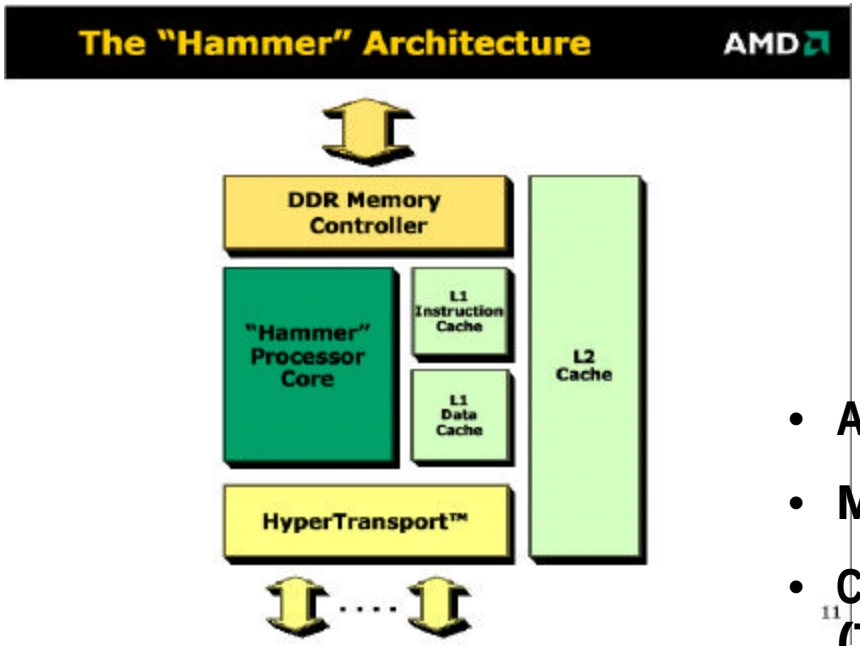
Agilent Technologies

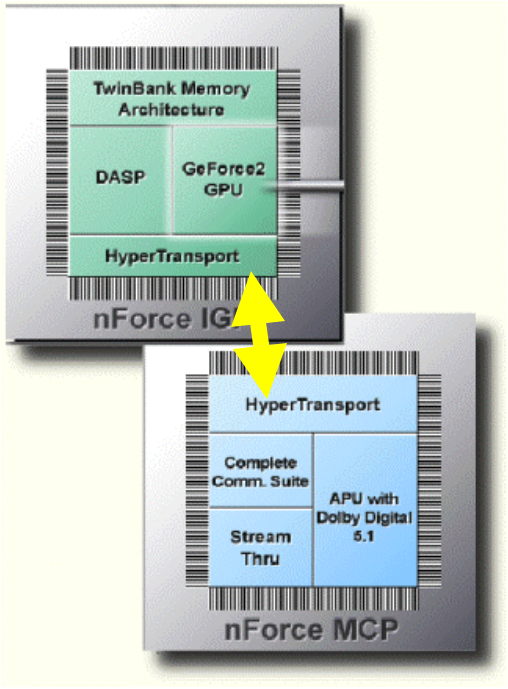
Content

- HyperTransport Overview
- HyperTransport Tests & Challenges
- High-Speed Source Synchronous Test
- Summary and Q&A

HyperTransport Technology Overview

- **Originally, HyperTransport was introduced by AMD**
- **Designed as high bandwidth solution for their next generation of Microprocessors.**

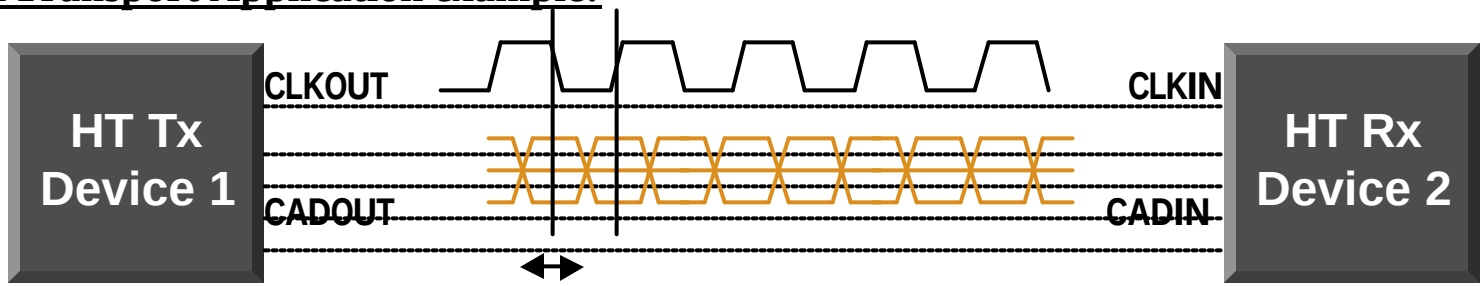




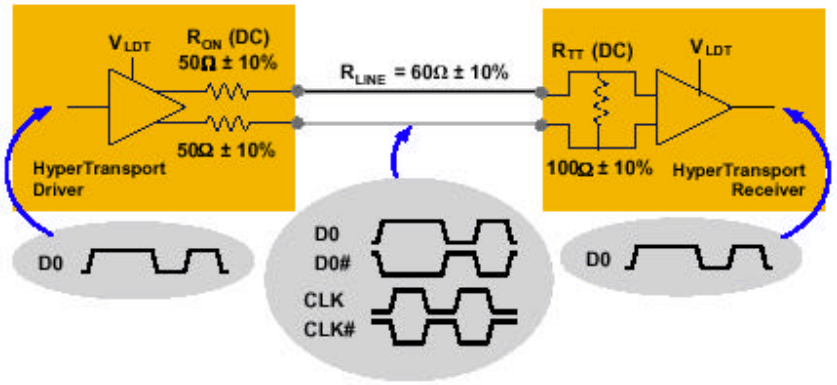
- **A HyperTransport consortium was founded**
- **Meanwhile, many companies has joined**
- **Companies from different market segments (Transmeta, SUN, Cisco, PMC-Sierra, Broadcom)**

What is HyperTransport?

HyperTransport Application example:



- **Scaleable I/O bus for high-speed operation**
  - **Bus Width: 2, 4, 8, 16, 32**
  - **Speed: 400Mbit ... 1.6 Gbit**
- **Designed for chip-to-chip link ('in the box')**
- **Differential, LVDS type signaling**
  - **Device Swing: Typ: 600 mV**
  - **Common Mode voltage: Typ: 600 mV**
- **Unidirectional bus (dedicated TX and RX lines)**
  - **100 Ohm Cross Termination**
  - **50 Ohm Driver Output Impedance**

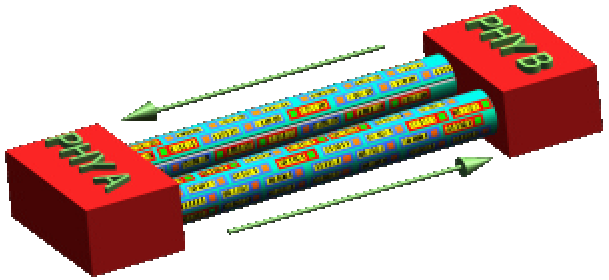


List of Different HyperTransport Parameters

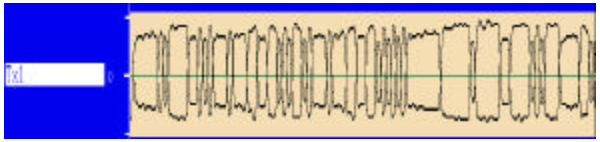
	PARAMETER	*DESCRIPTION*	*TESTED with 93K/P800*	*TESTED with NP1700*
Level:	Vod	Differential Output Voltage	YES	YES
	Vocm	Output common-mode voltage	YES	YES
	Vid	Differential Input Voltage	YES	YES
	Vicm	Input common-mode voltage	YES	YES
Impedance:	Rtt	Differential Input Impedance	YES	YES
	Ron	Driver Output Impedance	YES	YES
Timing:	**Tbit**	Bit Time 400 Mbps	YES	YES
		800 Mbps	YES	YES
		1.6 Gbps	-	**YES**
	Tcadv	Transmitter output Clock/Data	YES	YES
		skew	YES	YES
	Tsu	Receiver input setup time	YES	YES
	Tdh	Receiver input hold time	YES	YES
	TpIIIterror	**PLL long term phase error**	-	**YES**
	:	:		
	:	:		

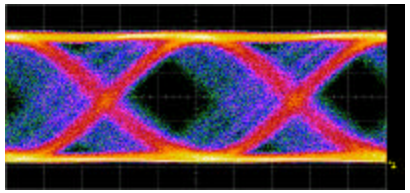
New Tester Capabilities

HyperTransport Test Challenges



LVDS!

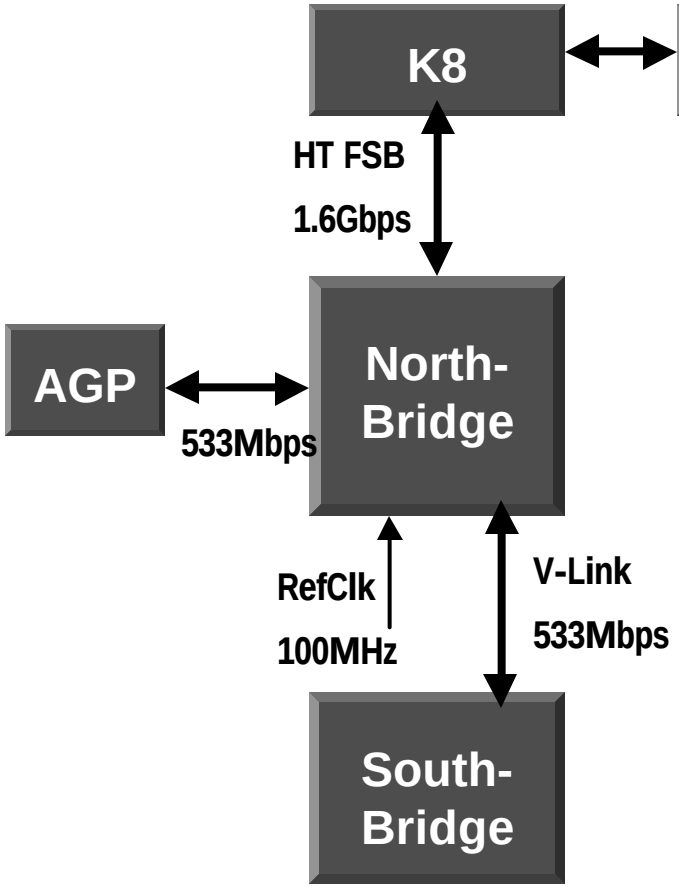




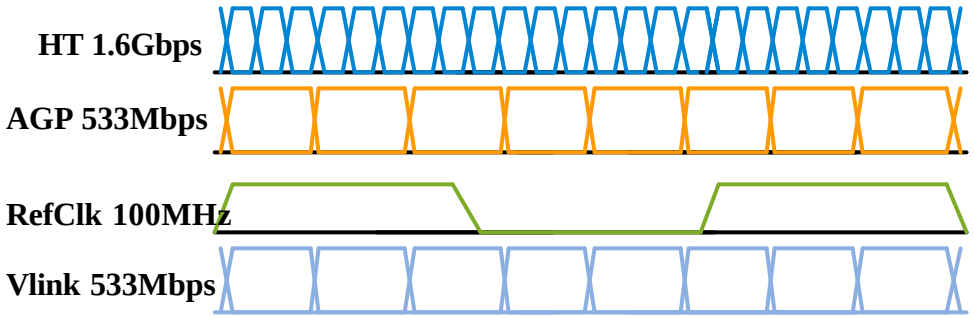
Source Sync!

- High Speed Data Rates up to 1.6 Gbit/s require Highest Speed and Accuracy
- Low Swing Differential Signals (DC/AC measurements)
- Debug & Characterize your High Speed Interface to bring your Device fast into production
- Source Synchronous bus interface

Application Example: North-Bridge Chip

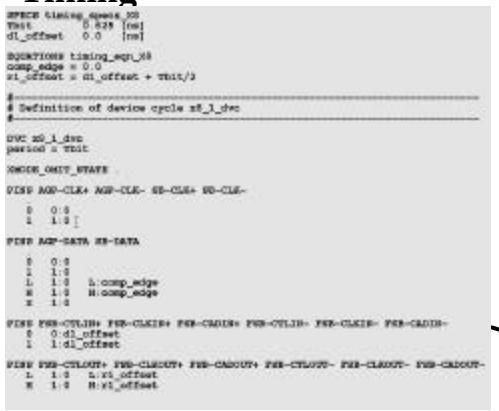


North-Bridge Timing:

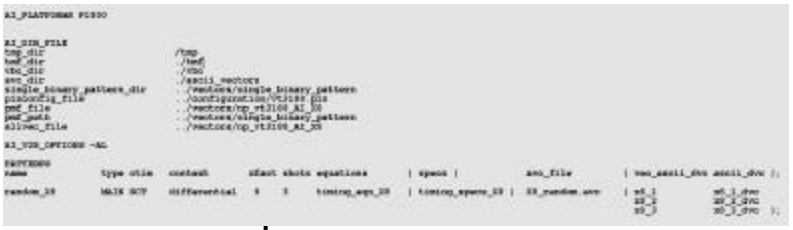


Application Example: North-Bridge Timing

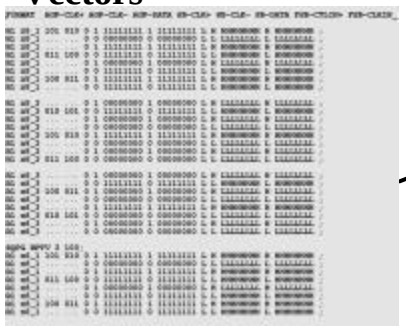
Timing



Configuration



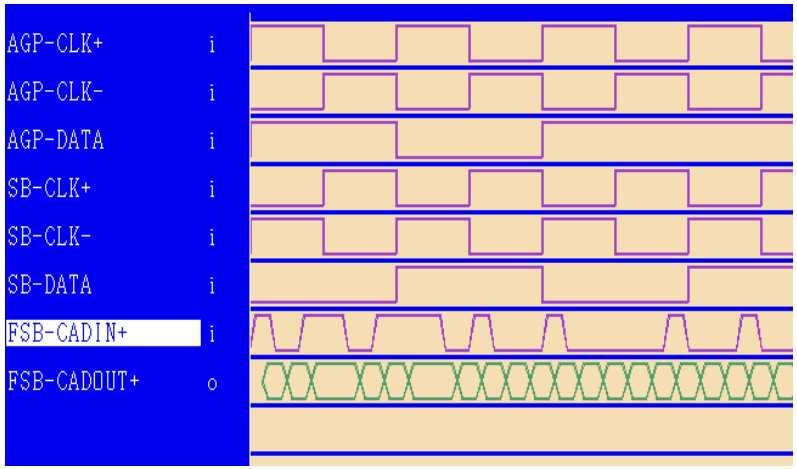
Vectors



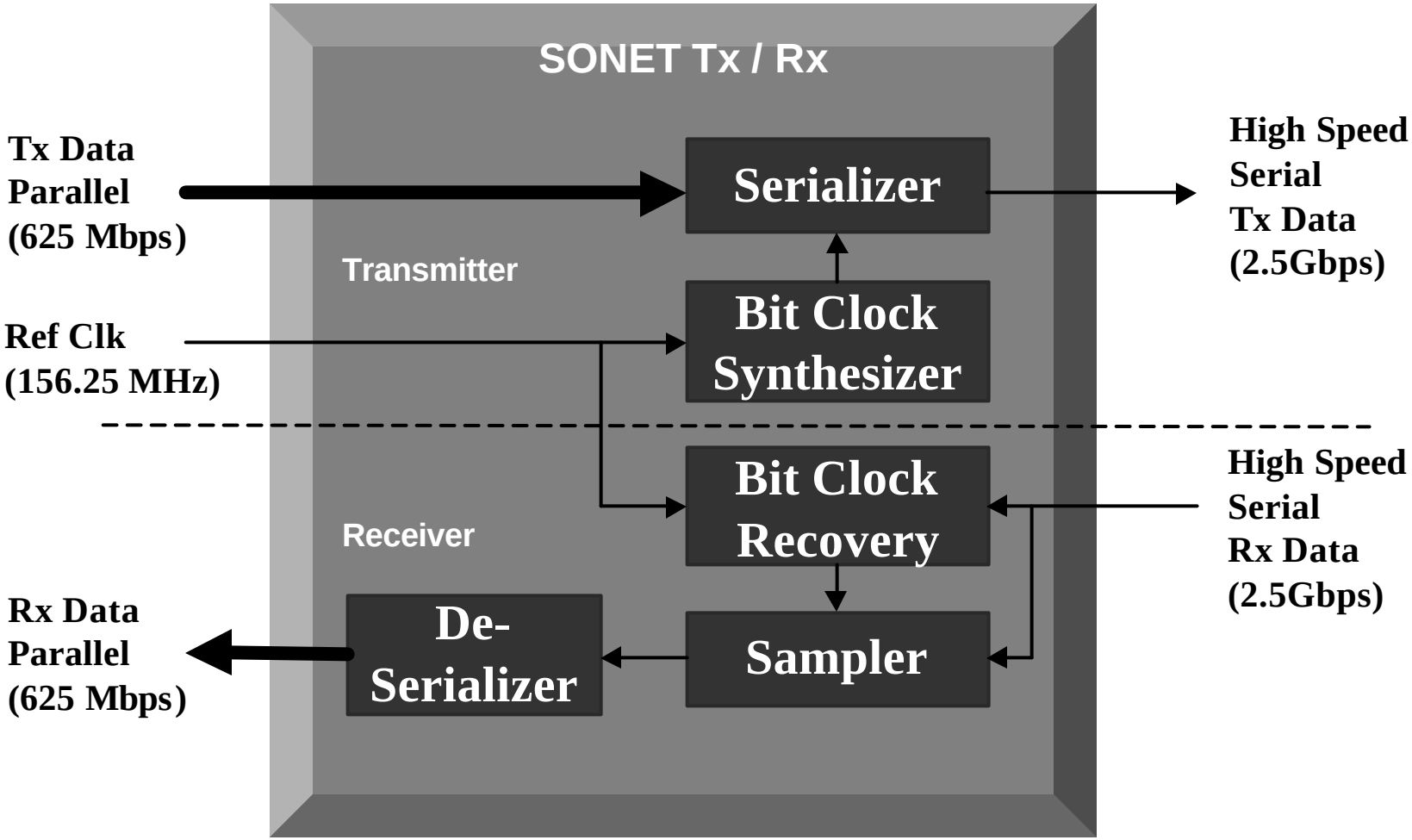
ASCII Interface

Combinations

```
#-------------------------------------------------------------------------------
# Definition of combination rules for x8_1_dvc
#-------------------------------------------------------------------------------

DDC x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc x8_1_dvc
PINS AGP-CLK+ AGP-CLK- SB-CLK+ SB-CLK-
    [01] . . [01] . . [01] .

PINS AGP-DATA SB-DATA
    [01] . . [01] . . [01] .
    [LHX] . . [LHX] . . [LHX] .

PINS FSB-CTLIN+ FSB-CLKIN+ FSB-CADIN+


PINS FSB-CTLOUT+ FSB-CLKOUT+ FSB-CADOUT+
```



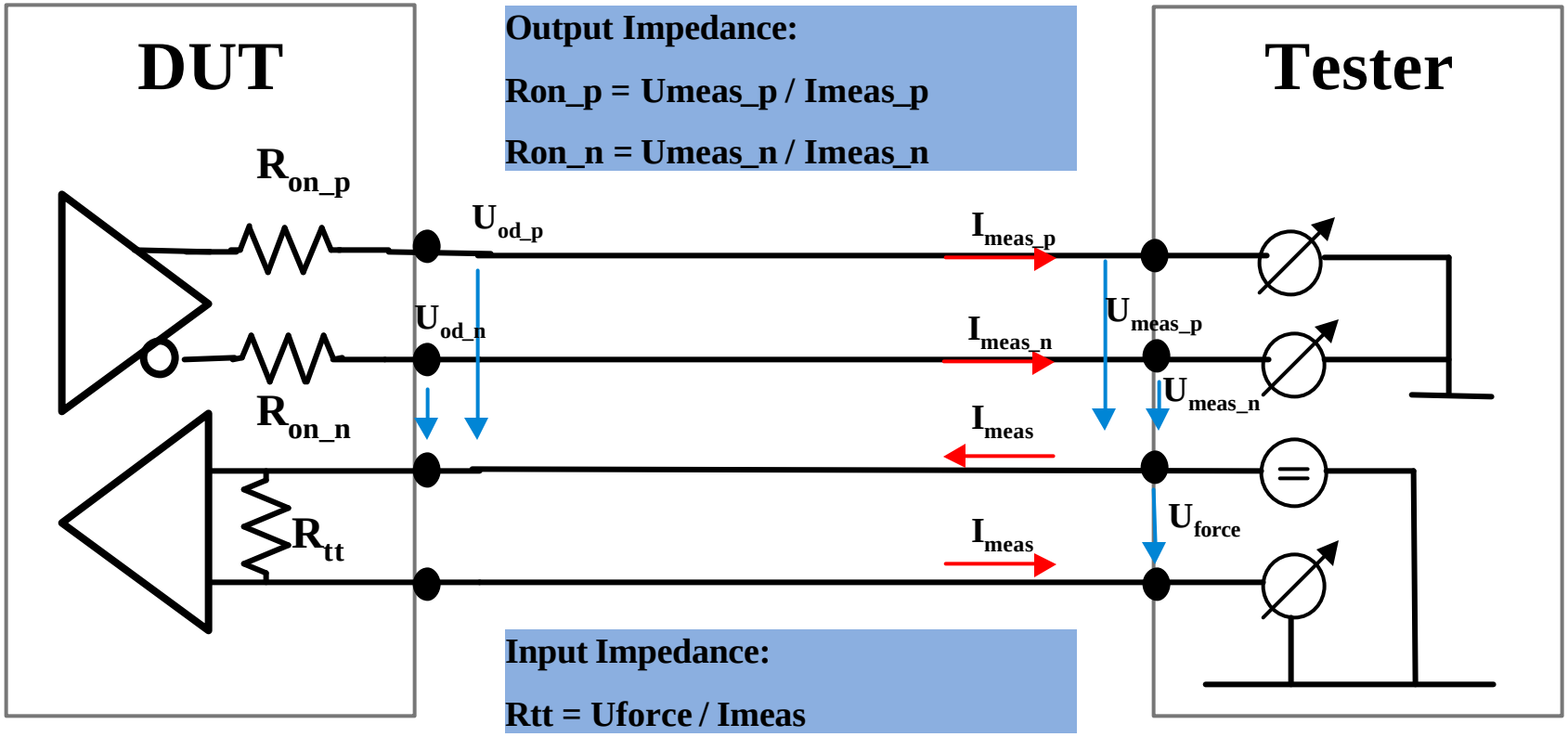
Application Example: SONET Chip (OC48)



Test List for High-Speed Interfaces

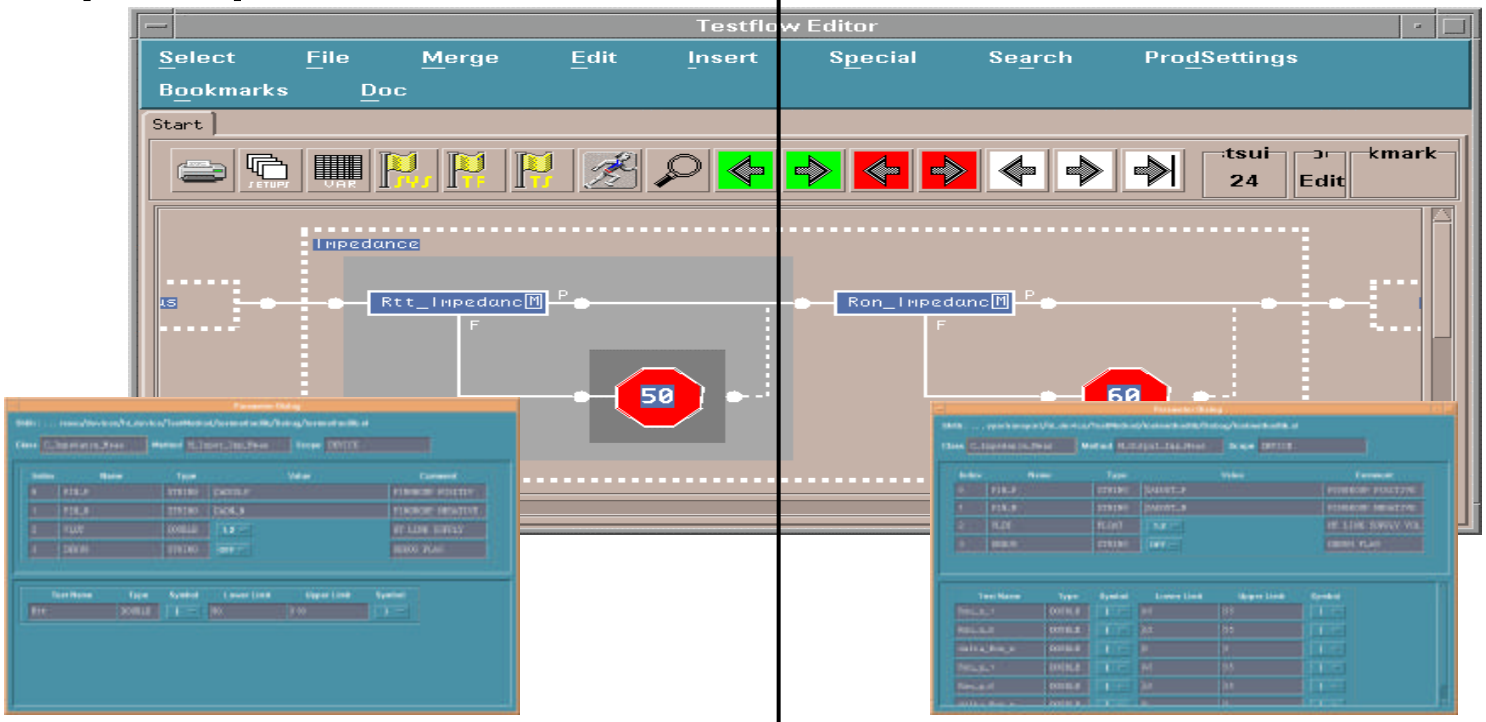
TEST LIST	*ATE NEEDS*
Impedance Test (Input, Output)	DC Access
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability
Receiver Skew Insertion	Timing Accuracy & Resolution
Transmitter Skew Measurements	Timing Accuracy, High Linearity
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth
Rise / Fall Time Measurements.	High Bandwidth, High Resolution
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy
Jitter Test	Low System Jitter, All Others
Source Synchronous Test	Source Synchronous Mode
HV Production Solution	Full Integrated Solution, High Throughput

Impedance Test: Theory



Impedance Test: Tester Setup

- **Input Impedance**
- **Output Impedance**

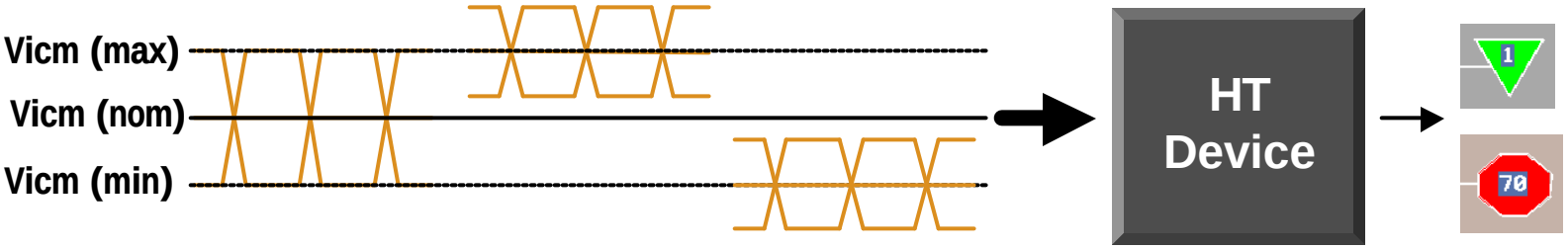


- **Pre-condition your device**
- **Force voltage: U_{force}**
- **Current measurement: I_{meas}**
- **Calculate Input Impedance: $R=U_{force}/I_{meas}$**
- **Pass / Fail decision**

- **Pre-condition your device**
- **DVM measurement: U_{meas}**
- **Current measurement: I_{meas}**
- **Calculate Input Impedance: $R=U_{meas}/I_{meas}$**
- **Pass / Fail decision**

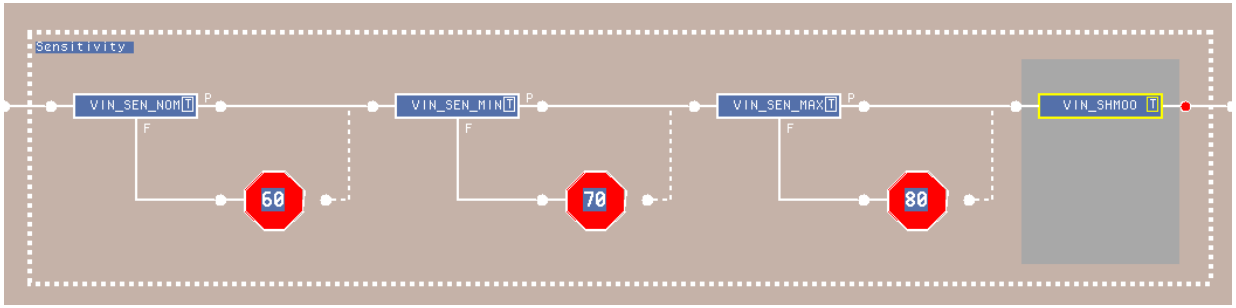
At Speed Receiver Test: Sensitivity Test

Input Sensitivity Test:



- For RX functional test, different level sets can be used to run at the specified limits
- Requires only one functional pattern to test the part to its limits

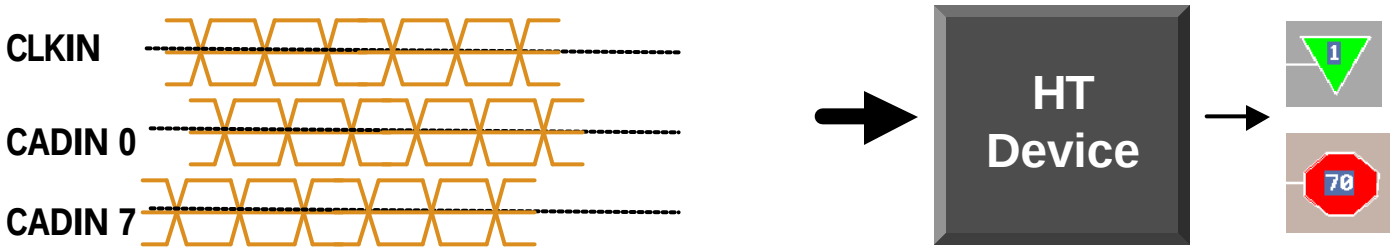
Tester Setup:




```
#####################################################################
# Equation Set for Level Sensitivity Test:
# Level Set 1:VLDT_NOM = 1.20V  VID_NOM = 600mV VICM_NOM = 600mV
# Level Set 2:VLDT_MIN = 1.14V  VID_MIN = 200mV VICM_MIN = 440mV
# Level Set 3:VLDT_MAX = 1.26V  VID_MAX = 1000mV VICM_MAX = 780mV
#####################################################################
EQNSET 2 "diff_level_eqn"

MODECONTEXT "differential"

SPECS
VLDT     [V]    # HyperTransport Link Supply Voltage
VID      [V]    # Input differential voltage
VICM     [V]    # Input common-mode voltage
I_LIMIT  [mA]

EQUATIONS
VIH = VICM + VID/2
VIL = VICM - VID/2

DPSPINS VTT
vout = VLDT
offcurr = act
ilimit = I_LIMIT
t_ms = 5

LEVELSET 1 "diff_tap_lset "

PINS CADIN_N CADIN_P
vil = VIL
vih = VIH

PINS CLKIN
vil = VIL
vih = VIH
```

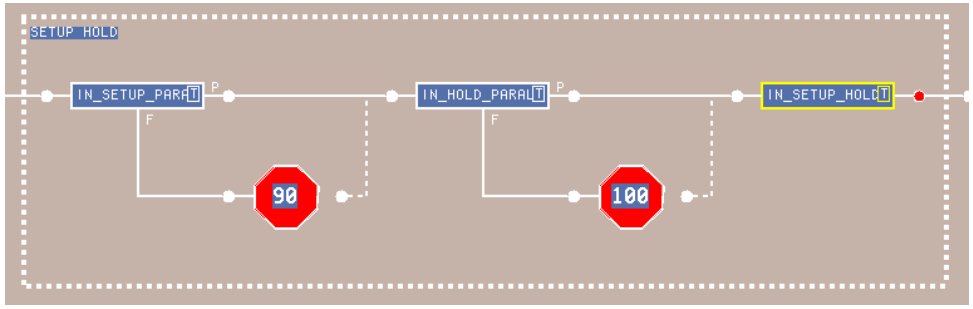
At Speed Receiver Test: Skew Insertion

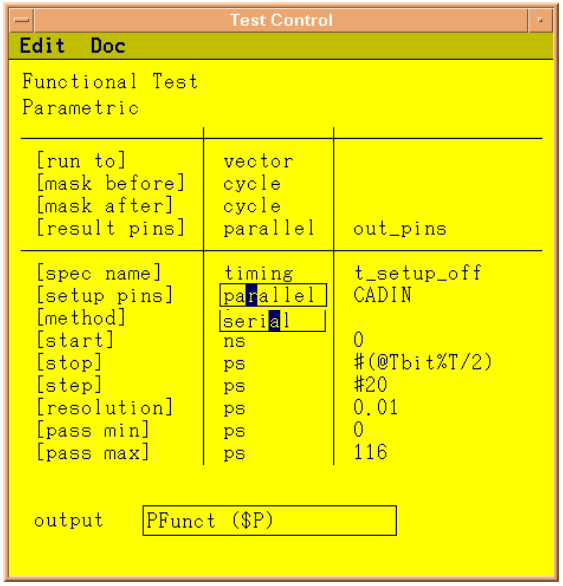
Input InterSkew Test:



- Program skew for all pins independently with spec variable
- Requires only one functional pattern to test the part to its limits

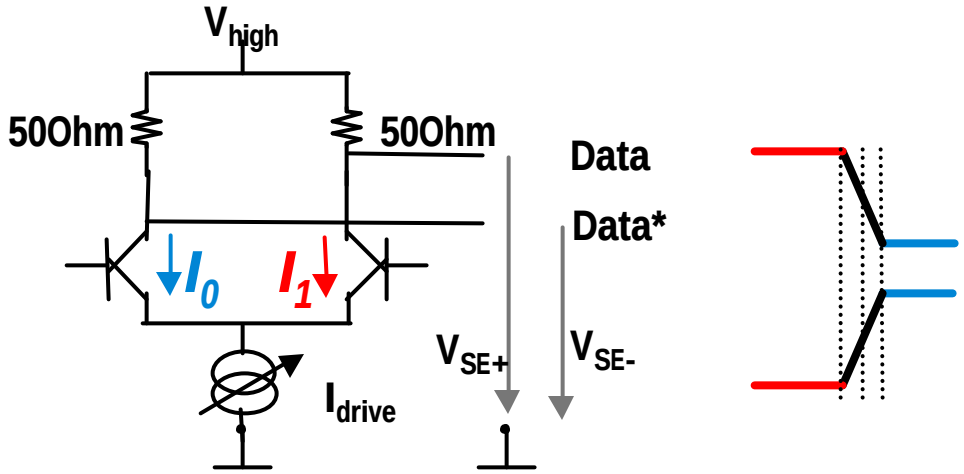
Tester Setup:

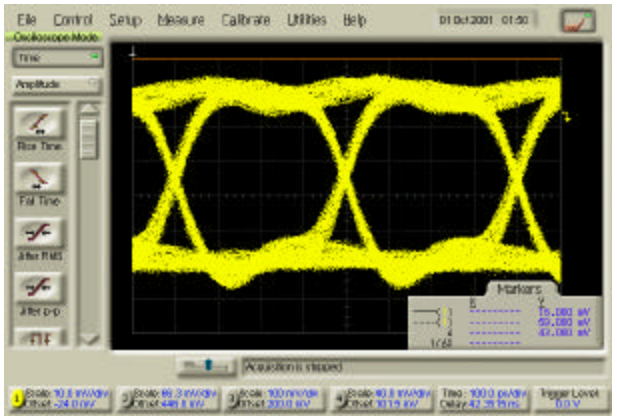




NP-Model Native Differential Driver

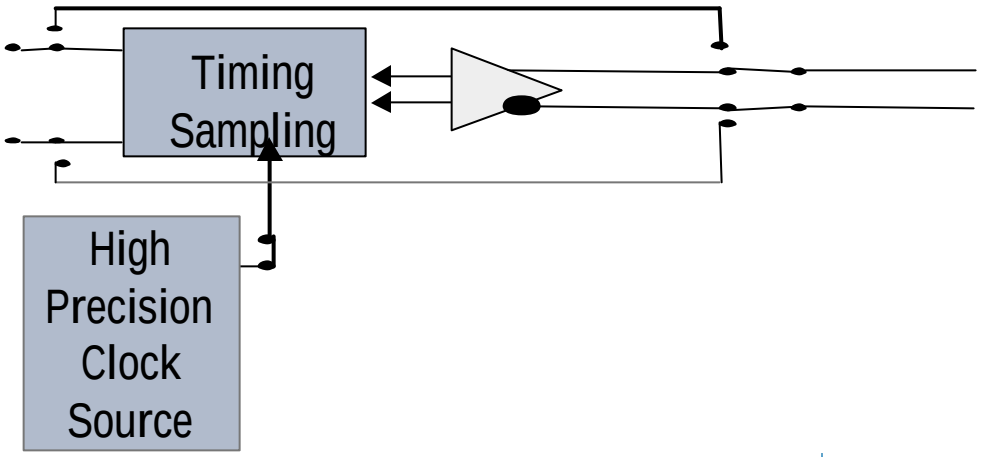
Differential Driver: Current Switch





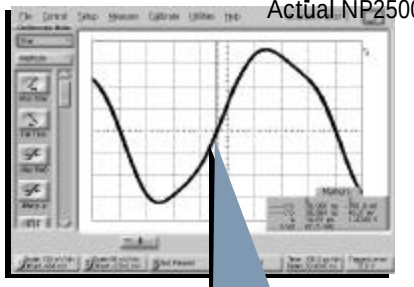
PRBS: 2.5 Gbps, 50 mV Swing

Retiming Unit:



NP2500 2.5 Gbps

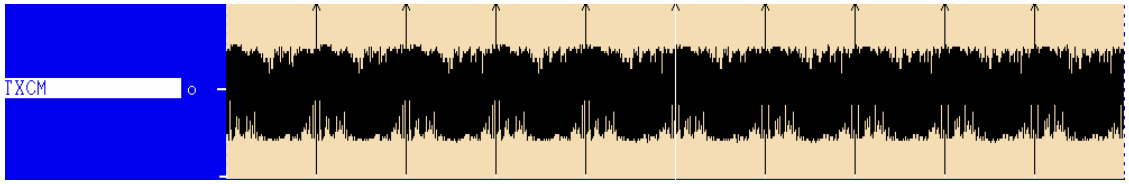
Actual NP2500 results

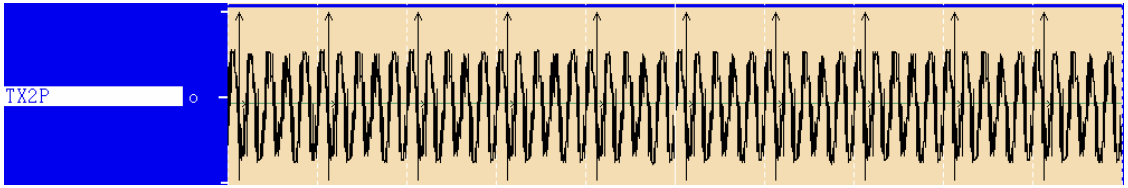


<2.5 ps Jitter

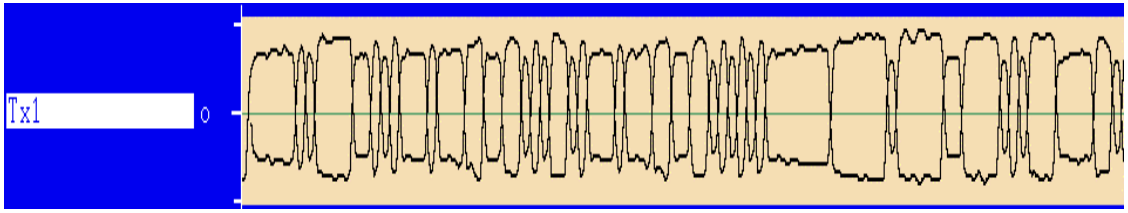
Fast Debug with Timing Diagram

- PLL is not locked





- Device Jitter
- Level verification
- Timing verification

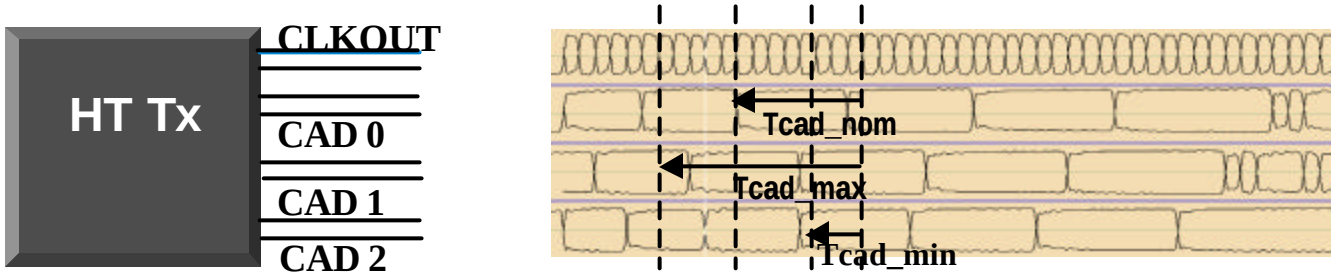


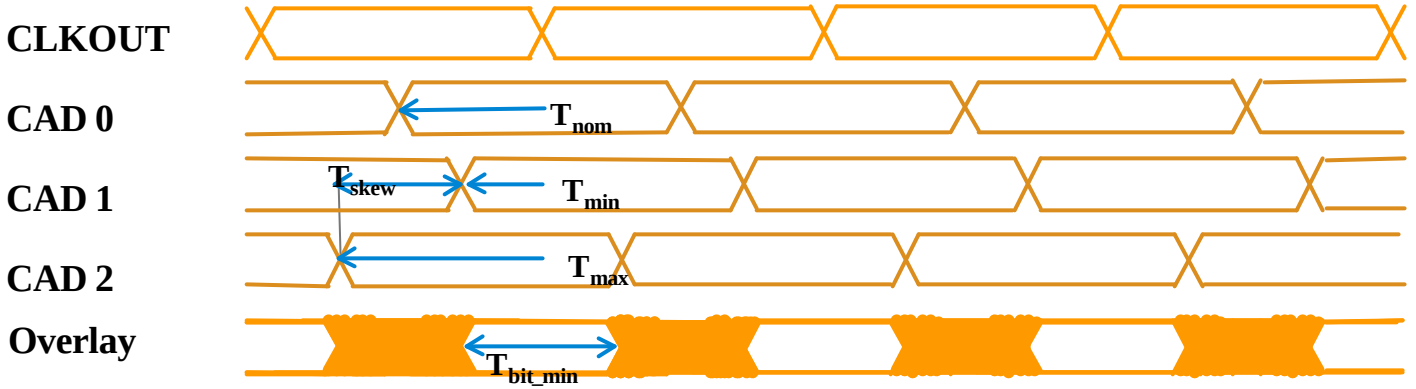
- Crossover Symmetry
- Pattern verification
- Common mode shift, Cross Talk, and many more

Fast Visual Feedback-Over a Wide Range!

Clock-Data Output Skew: Theory

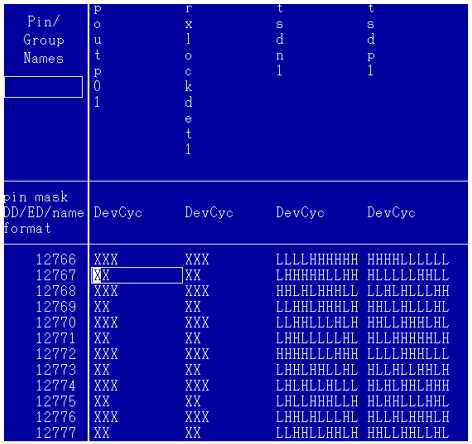
Device Output:



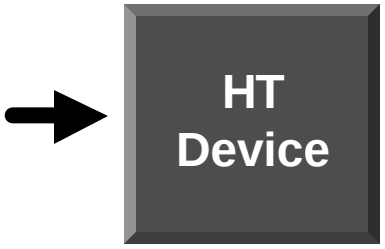


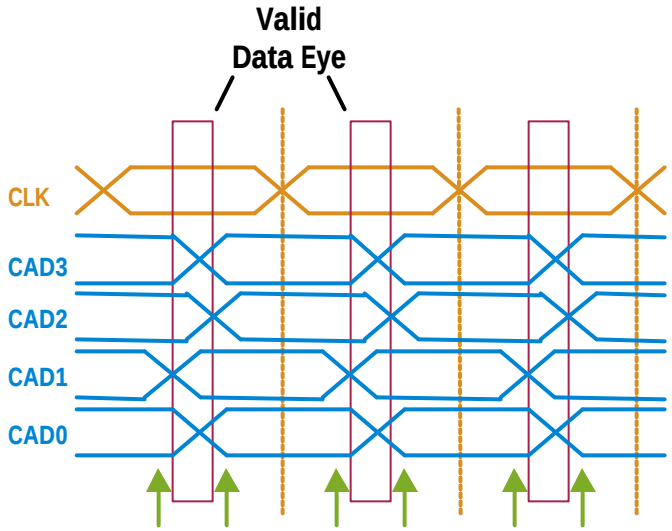
- T_{nom} = Nominal setup time between Clock and Data/Control
- T_{min} = Minimal setup time
- T_{max} = Maximal setup time
- T_{skew} = Maximal skew between data line T_{max} - T_{min}

At Speed Transmitter Test: Functional



Pin/ Group Names	pout p0 1	rxlock det 1	tsdn 1	tsdp 1
pin mask OD/BD/name format	DevCyc	DevCyc	DevCyc	DevCyc
12766	XXX	XXX	LLLLHHHHHH	HHHHLLLLLL
12767	XX	XX	LHHHHHLLHH	HLLLLLHHLL
12768	XXX	XXX	HHLHLHHHLL	LLHLHLLLHH
12769	XX	XX	LLHHLHHHLH	HHLLHLLLHL
12770	XXX	XXX	LLHHLLLHLH	HHLLHHHLHL
12771	XX	XX	LHHLLLLLHL	HLLHHHHHLH
12772	XXX	XXX	HHHHLLLHHH	LLLLHHHLLL
12773	XX	XX	LHHLHHLLHL	HLLHLLHHLH
12774	XXX	XXX	LHLHLLHLLL	HLHLHHLHHH
12775	XX	XX	LHLLHHHLLH	HLHHLLLHHL
12776	XXX	XXX	LHHLHLLLHL	HLLHLHHHLH
12777	XX	XX	LLHHLLHHLH	HHLLHHLLHL

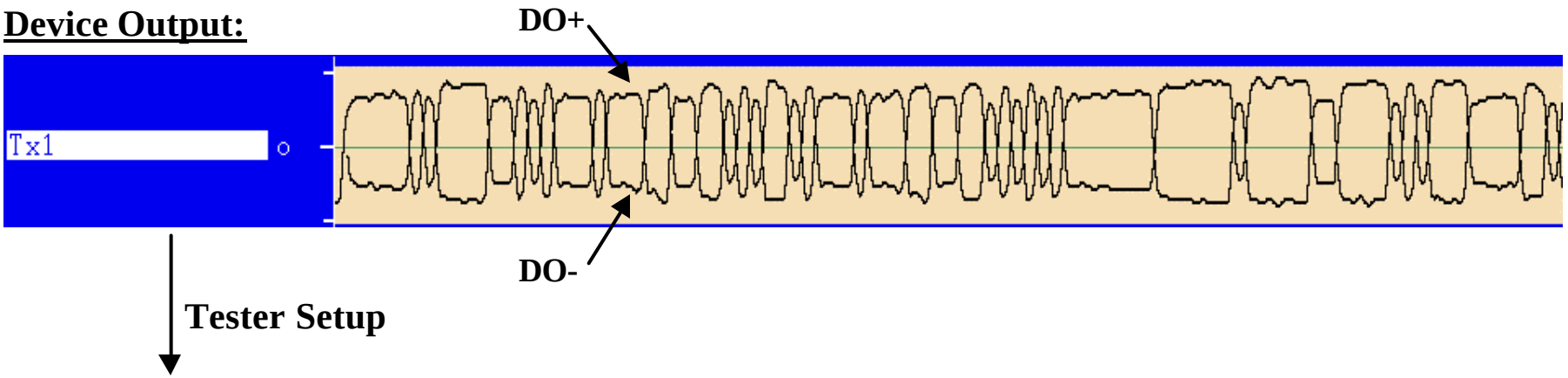




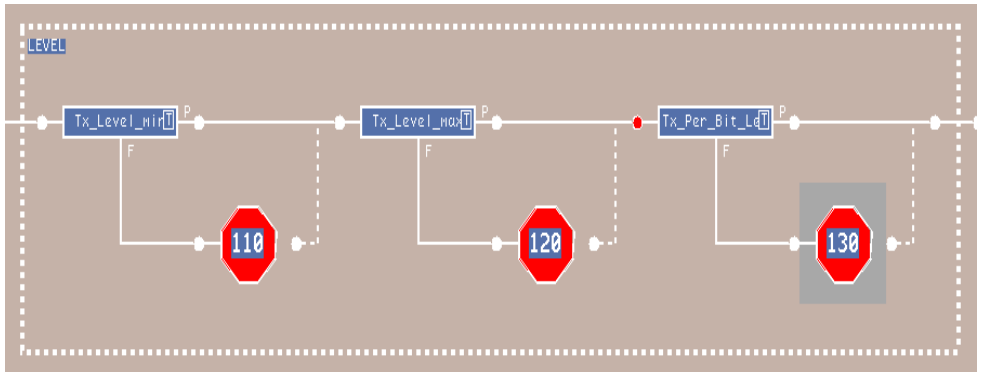
- Search the clock edge (Tclk) and
- Program relative to the Tclk the edge delays
- Tvalid = Tbit - 2*Tcad_min
- Apply a large pattern to guaranty worst-case output skew.

At Speed Transmitter Test: Voltage

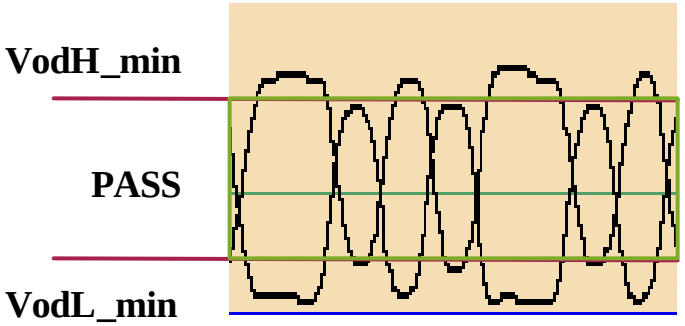
Device Output:



Testflow:

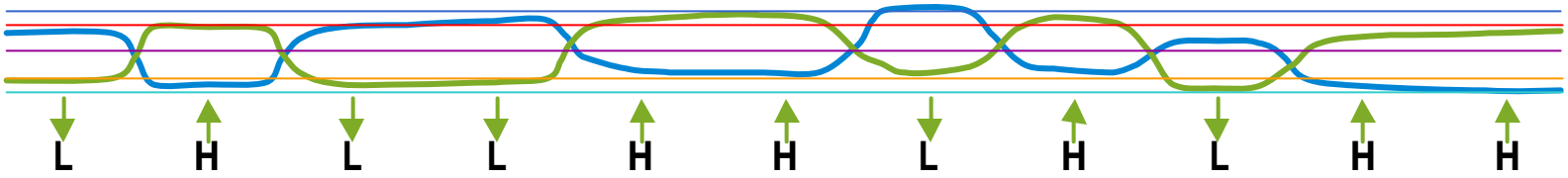


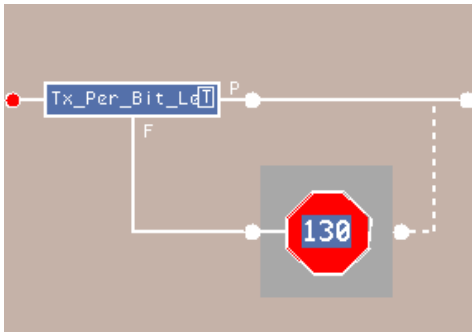
Minimum Output Voltage:



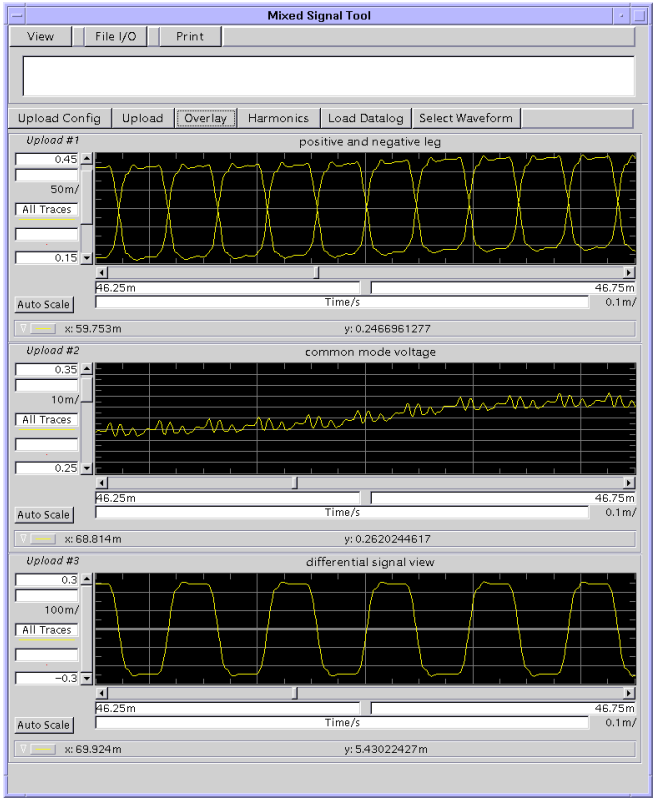
•Measure over a large number of samples to measure worst-case output voltage.

Per Bit Voltage Measurement

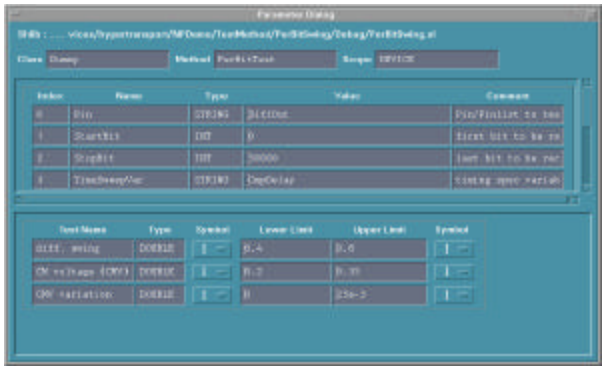




Overlay of N and P Out



Output Vcom



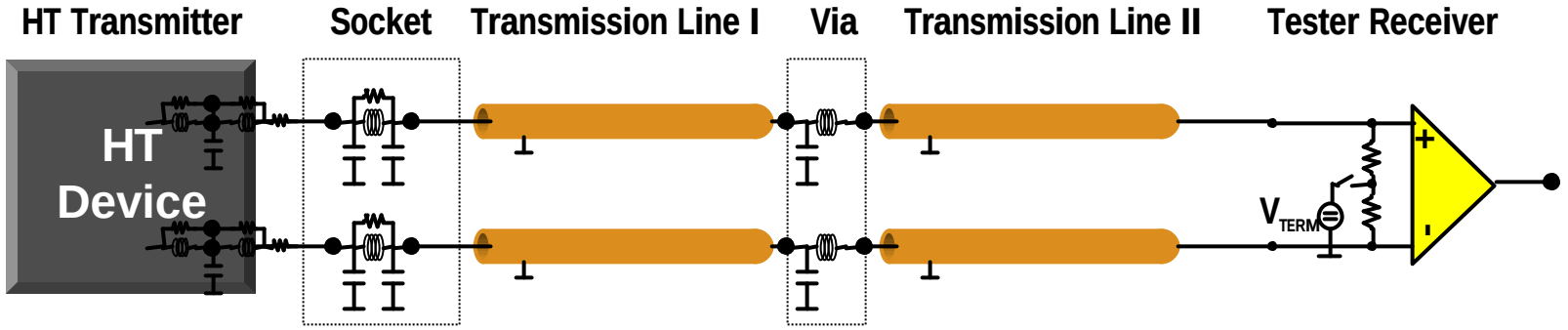
Output Vswing

Summary

TEST LIST	*ATE NEEDS*	*COVERED*
Impedance Test (Input, Output)	DC Access	✓
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability	✓
Receiver Skew Insertion	Timing Accuracy & Resolution	✓
Transmitter Skew Measurements	Timing Accuracy, High Linearity	✓
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth	✓
Rise / Fall Time Measurements.	High Bandwidth, Resolution, Low Overdrive	
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy	
Jitter Test	Low System Jitter, All Others	
Source Synchronous Test	Source Synchronous Mode	
HV Production Solution	Full Integrated Solution, High Throughput	✓

Rise / Fall Time Measurements: Theory

Transmission Path:



$$T_{composite} = \sqrt{T^2_{r\_device} + T^2_{r\_package} + T^2_{r\_socket} + T^2_{r\_via} + T^2_{r\_cable} + T^2_{r\_BW}}$$

DUT_Board considerations:

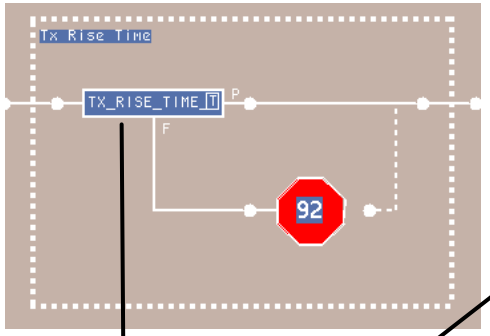
- Uniform trace impedance across the whole trace (reflections)
- Vias and other potential impedance discontinuities should be minimized (reflections)
- Make your trace width as wide as possible (skin effect)
- Talk to your PCB manufacturer about modeling techniques used

More Details:

- Hall, Hall, McCall: “High-Speed Digital System Design”
- Johnson, Graham: “High-Speed Digital Design”

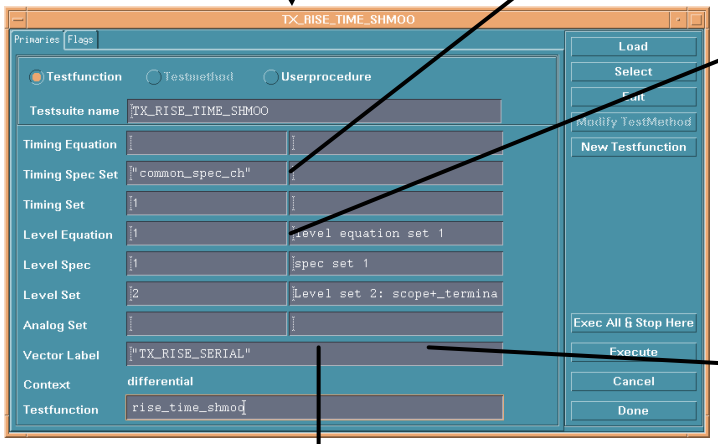
Rise / Fall Time Measurements: Setup

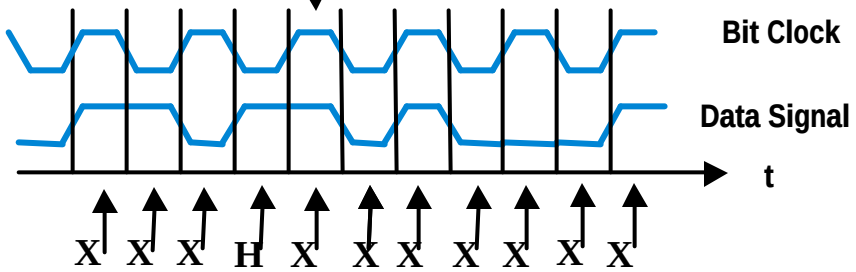
Testflow:

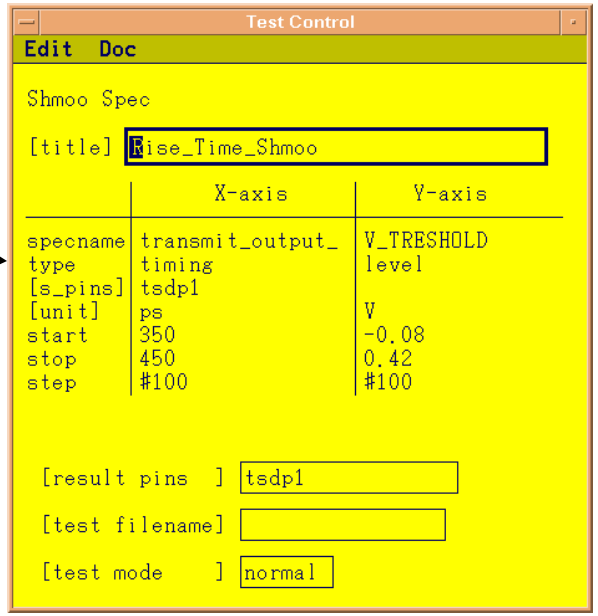



```
PINS  tsdp1
# USED WAVEFORMS 0 1 2 3 4 5 6 7 8 9 a b c d e f 10
15 16 17 18 19 1a 1b 1c 1d 1e 1f
r1=time_ps*transmit_output_strobe + Tx1_offset #RU
```

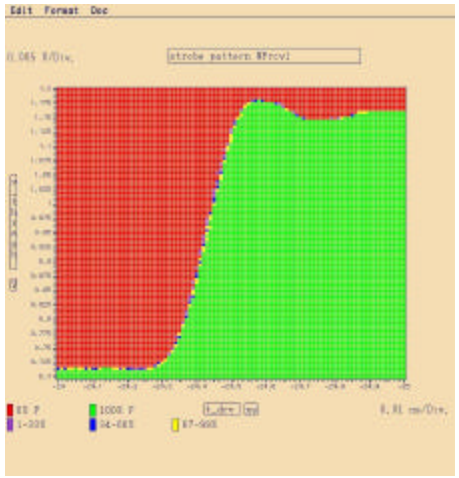
```
PINS tsdp1 tsdn1
term scope+
vt = CML_swing/2
vth = V_TRESHOLD
```





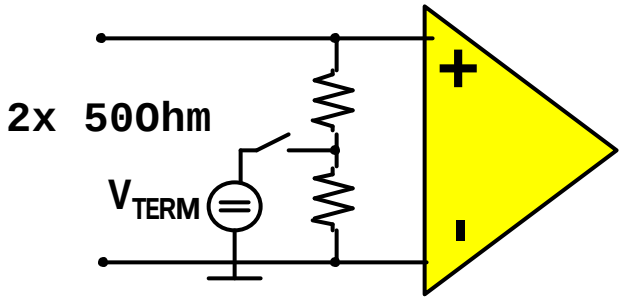


Rise / Fall Time Measurements: Results



120 ps Rise Time
@400 mV Swing
@ the Receiver!

Differential Comparator



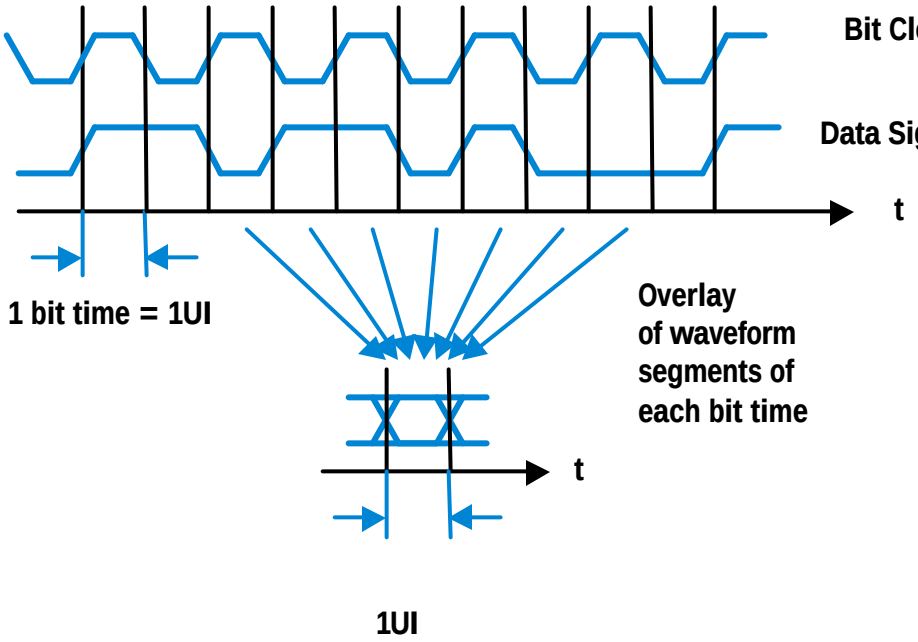
The Receiver matches the Application

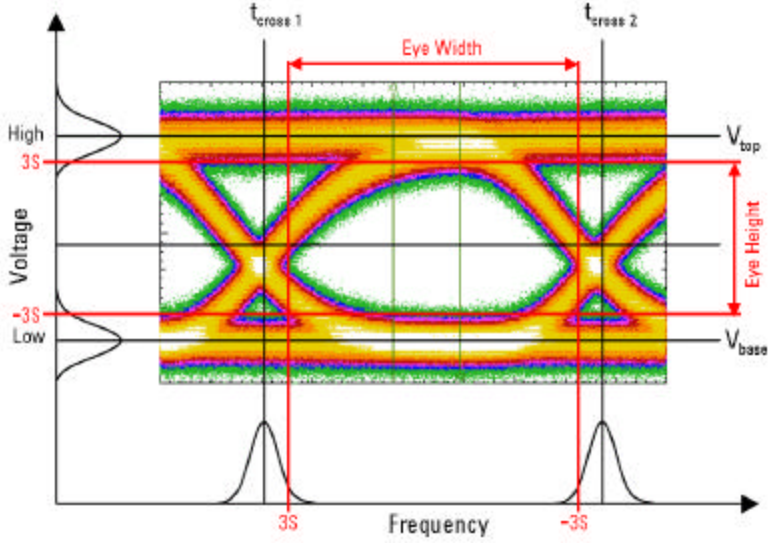
- True differential
- Floating (and center tap) termination
- Outstanding bandwidth
- Built-in scope capability up to 2.5 Gbps

Debug and Test the REAL DUT output!

Eye Diagram: Theory

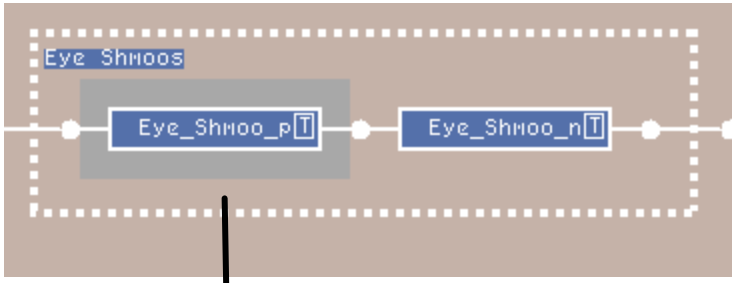
Eye diagram is an overlay of many waveforms recorded with a bit clock as a trigger. This is a important parametric characteristics of the high speed transmit interface. Rise time / Fall time, jitter, and signal levels, overshoot, undershoot, ripple can be extracted from an eye diagram.

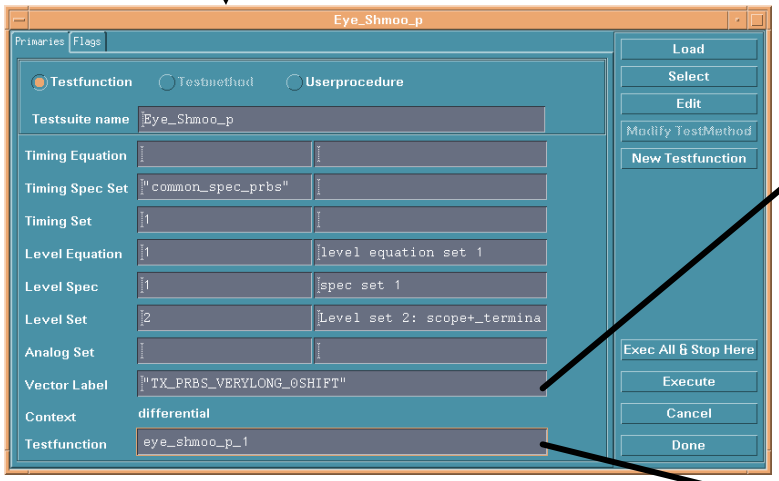


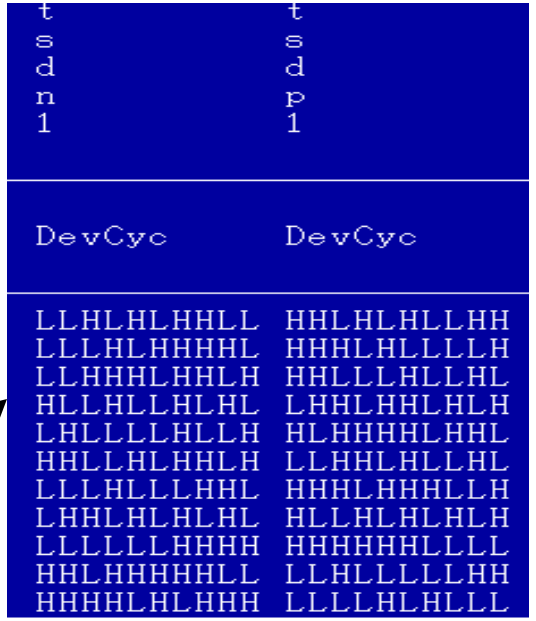


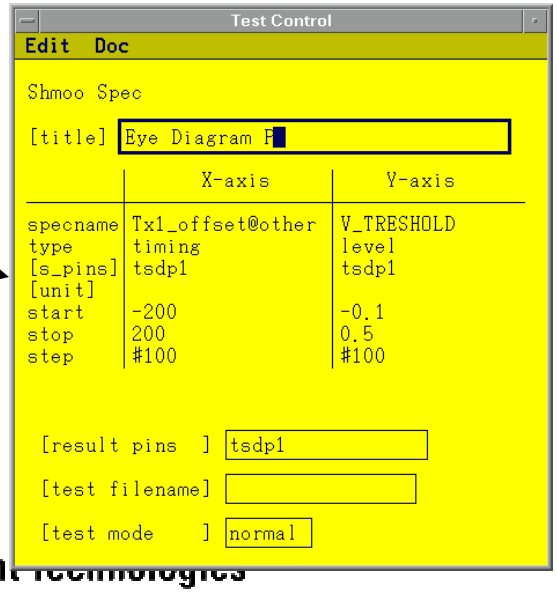
Eye Diagram: Setup

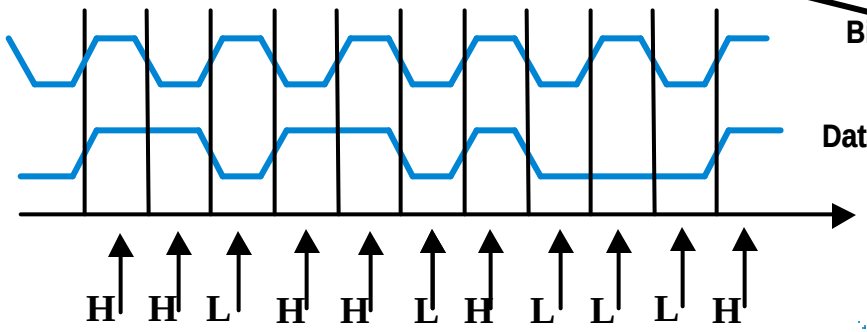
Testflow:











Bit Clock

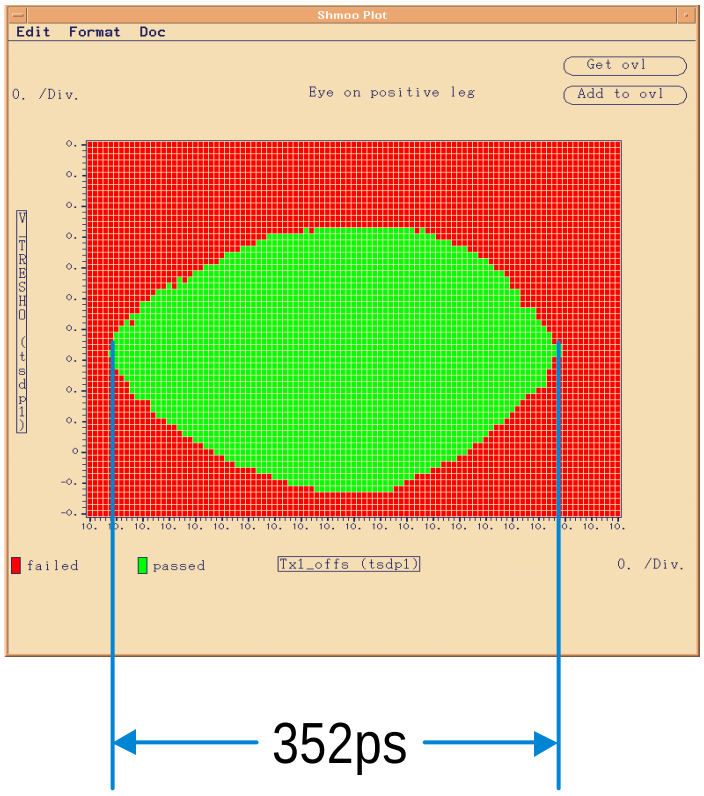
Data Signal

t

Eye Diagram: Results I

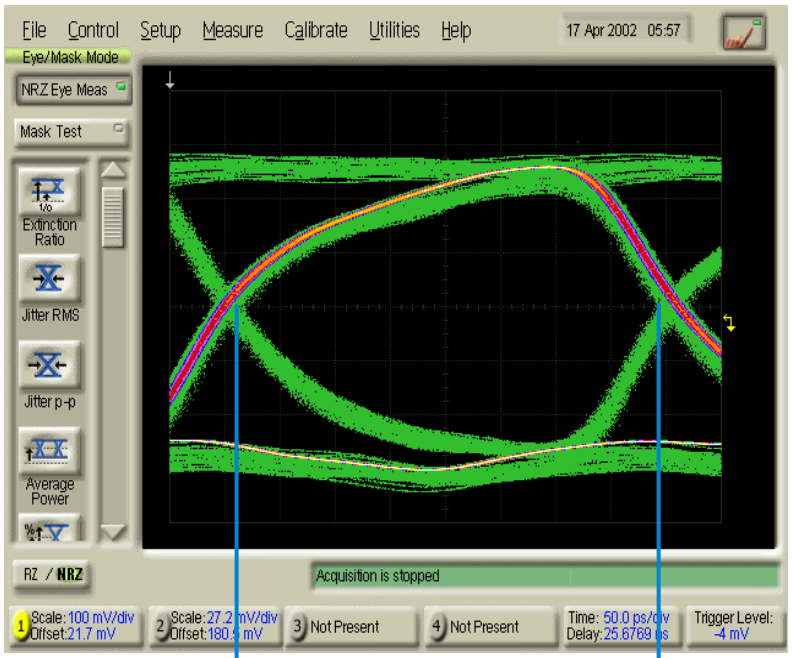
Real Device Out @ 2.5 Gbps:

Eye Shmoo:



352ps

DCA:

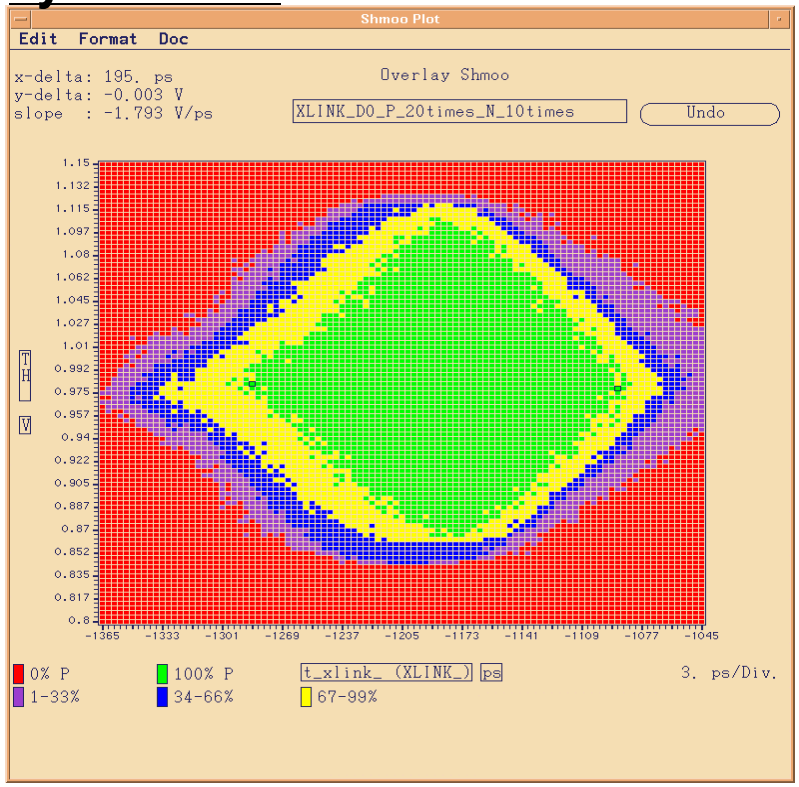


350.5ps

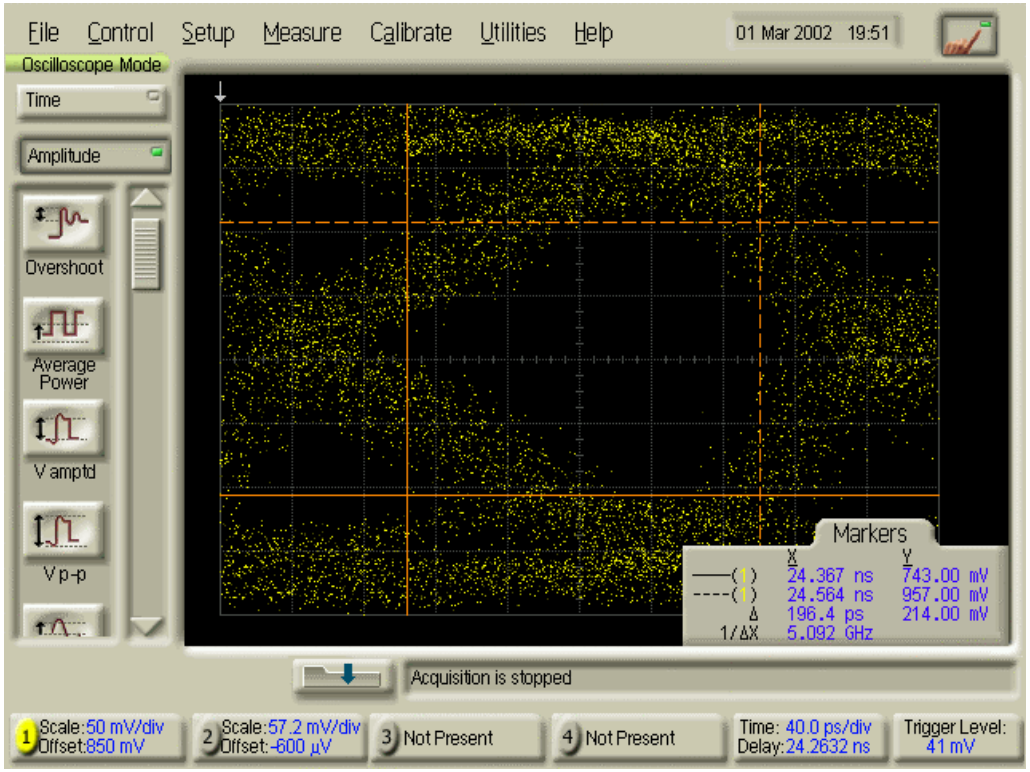
Eye Diagram: Results II

Real Device Out @ 3.125 Gbps:

Eye Shmoo:



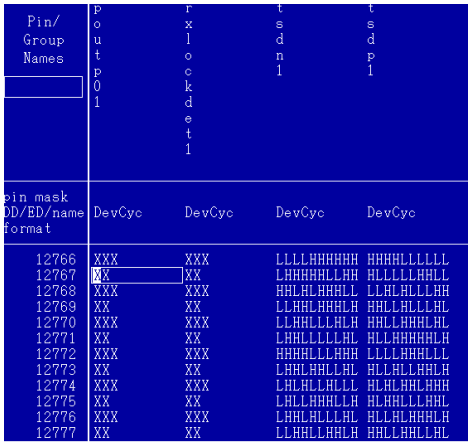
DCA:



See the REAL DUT output!

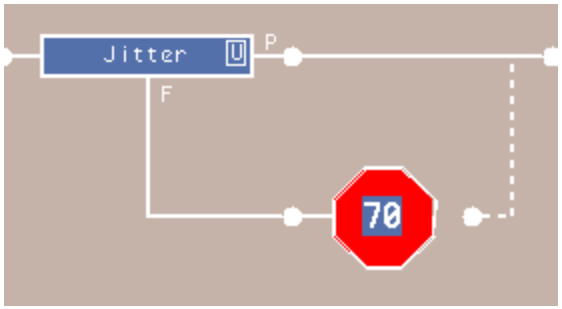
Jitter Measurements

1)Apply PRBS Pattern

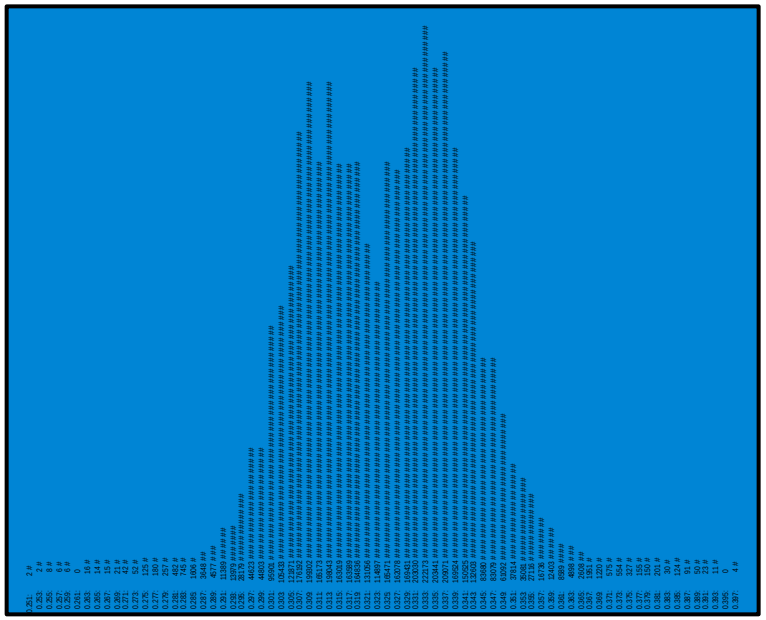


Pin/ Group Names	p o u t p 0 1	r x l o c k d e t 1	t s d n 1	t s d p 1
pin mask DD/ED/name format	DevCyc	DevCyc	DevCyc	DevCyc
12766	XXX	XXX	LLLLHHHHHH	HHHHLLLLLL
12767	XX	XX	LHHHHHLLHH	HLLLLLHHLL
12768	XXX	XXX	HHLHLHHHLL	LLHLHLLLHH
12769	XX	XX	LLHHLHHHLH	HHLLHLLLHL
12770	XXX	XXX	LLHHLLLHLH	HHLLHHHLHL
12771	XX	XX	LHHLLLLLHL	HLLHHHHHLH
12772	XXX	XXX	HHHHLLLHHH	LLLLHHHLLL
12773	XX	XX	LHHLHHLLHL	HLLHLLHHLH
12774	XXX	XXX	LHLHLLHLLL	HLHLHHLHHH
12775	XX	XX	LHLLHHHLLH	HLHHLLLHHL
12776	XXX	XXX	LHHLHLLLHL	HLLHLHHHLH
12777	XX	XX	LLHHLLHHLH	HHLLHHLLHL

2)Measurements & Calculation



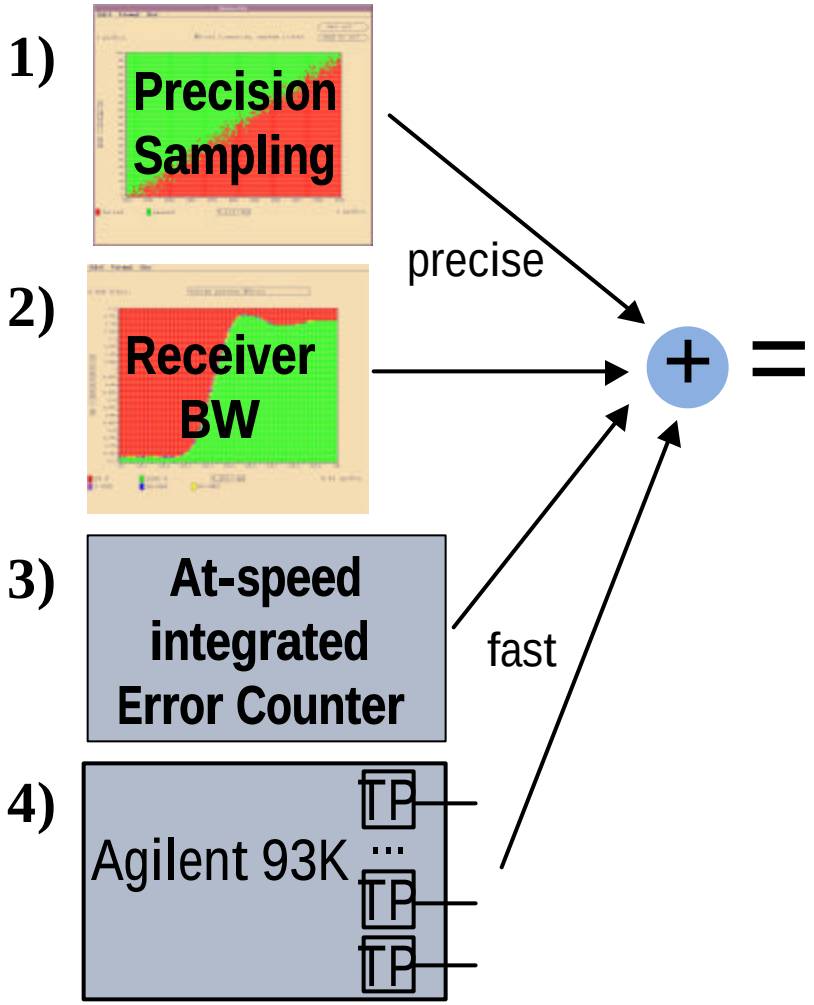
3) Histogram

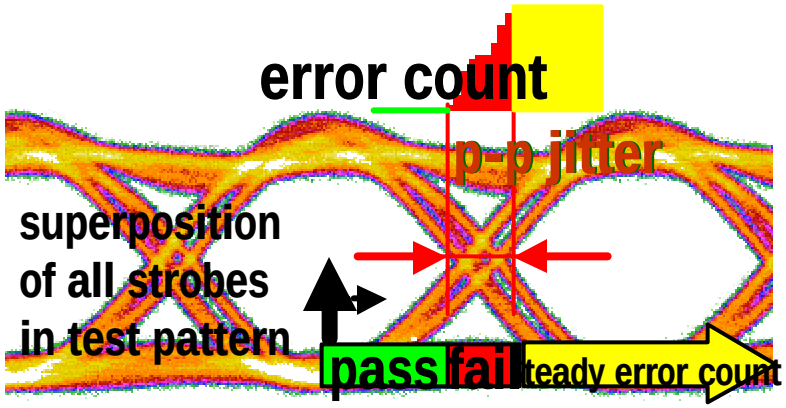


- Jitter Test at full speed on a PRBS Pattern
- Returns PP & RMS Value, etc.
- Real-time compare without capture & upload
- No additional instrument needed

Identify Your Device Jitter FAST!

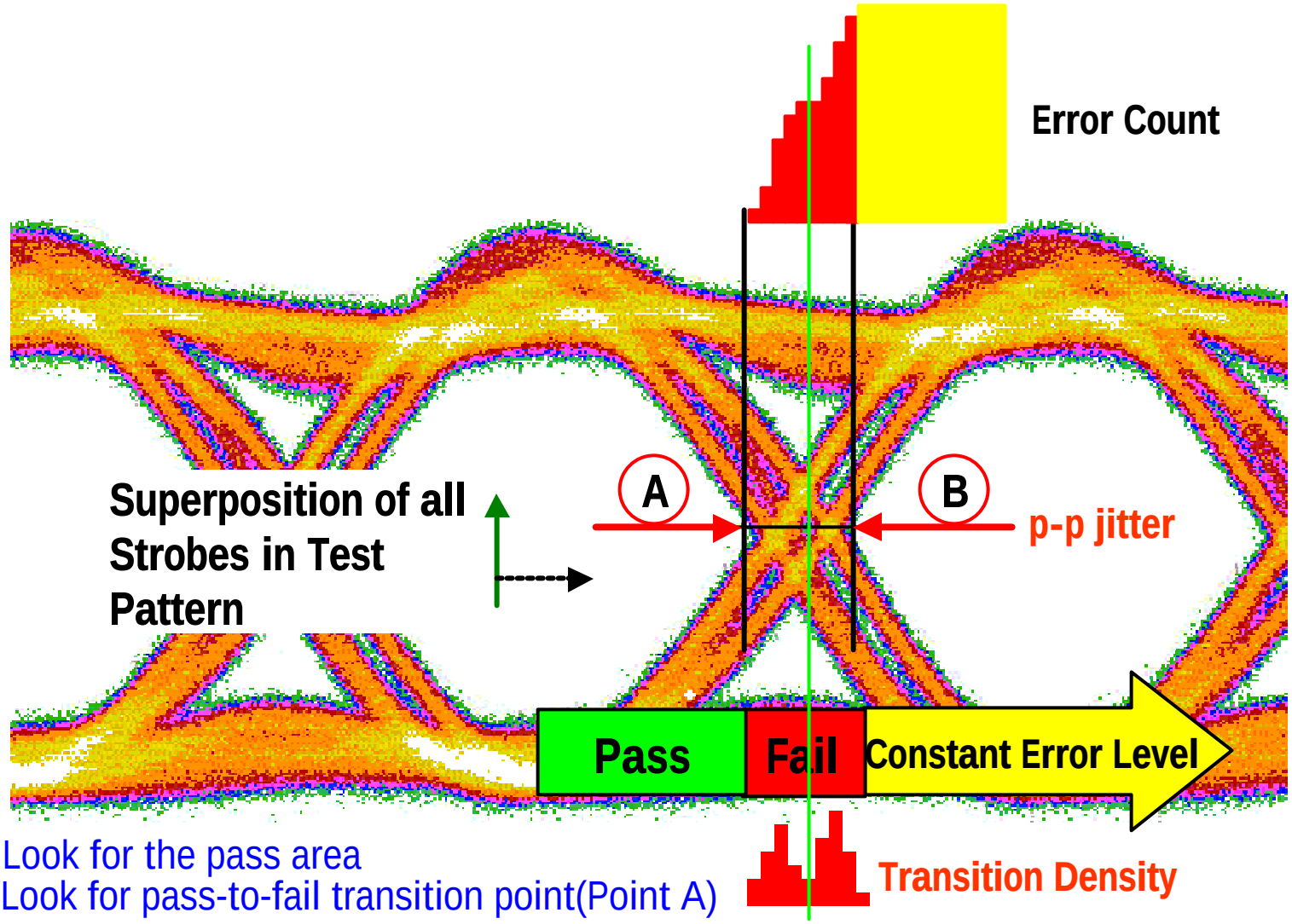
Ultra Fast Jitter Measurements





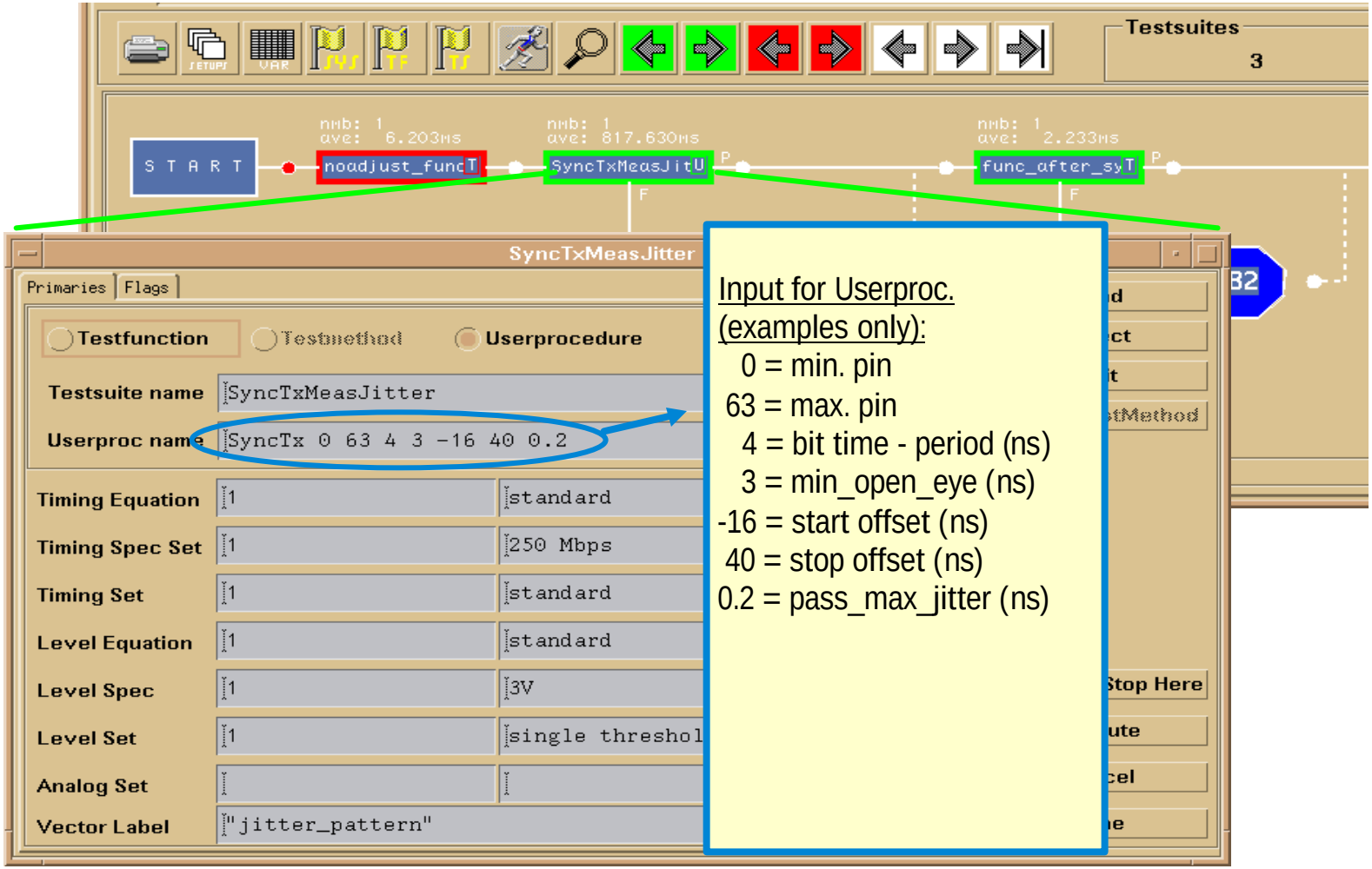
- Highly linear timing delay circuits per pin (5ps)
- Resolution down to 1 ps
- Superior comparator bandwidth
- Test Processor-Per-Pin Architecture for PARALLEL execution
- Error Counter

Jitter Measurement: Theory

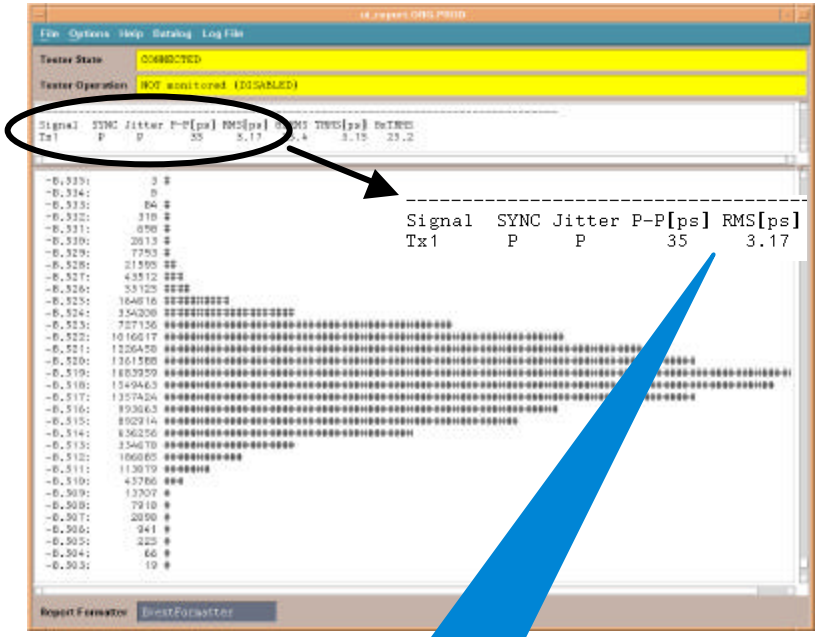


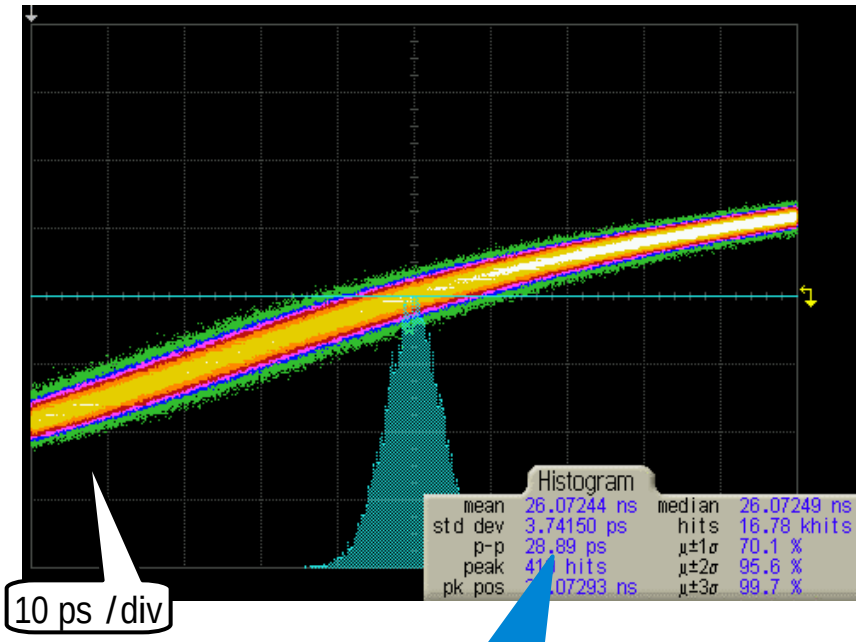
1. Look for the pass area
2. Look for pass-to-fail transition point(Point A)
3. Use 93K Error Count feature to look for max error count, take it as Point B
4. The time difference between Point A & Point B is considered as peak-to-peak jitter

Implementation



Measurement Results: SerDes Device with Clock Signal

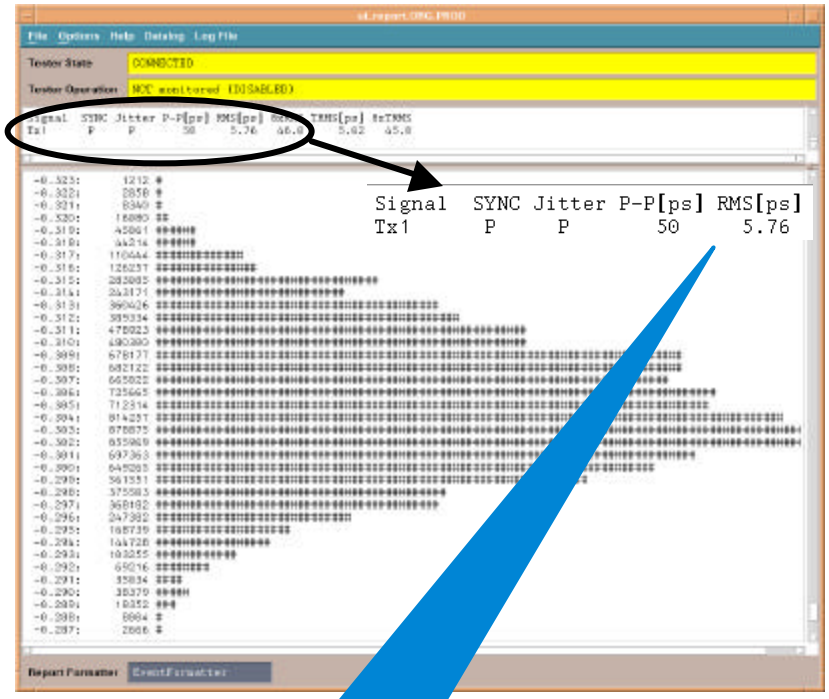




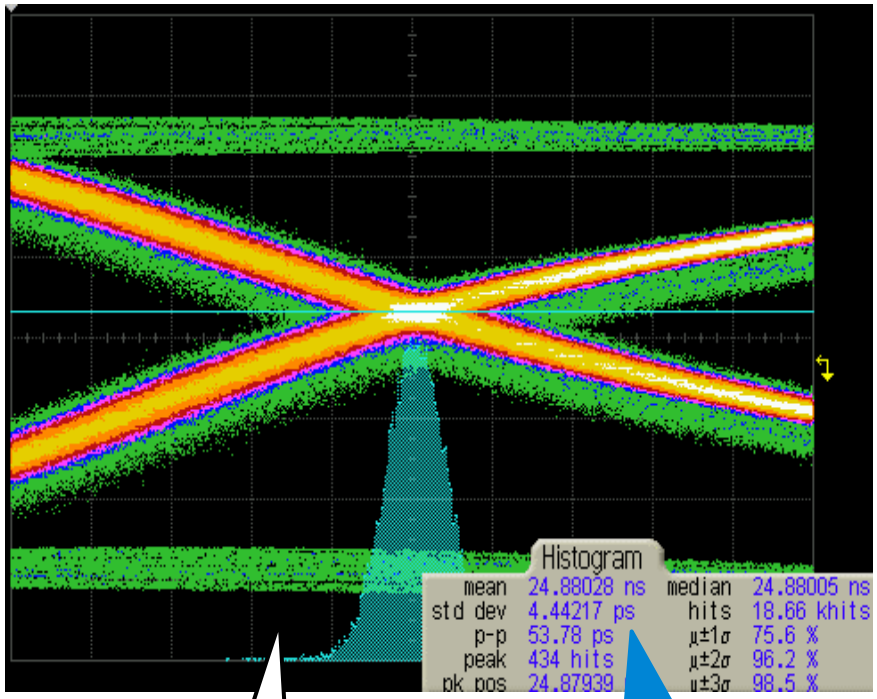
Random Jitter
35 ps p-p
3.57 ps RMS

Random Jitter:
28.9 ps p-p
3.74 ps RMS

Measurement Results: SerDes Device with Data Pattern (DDJ + RJ)



50 ps p-p Jitter!

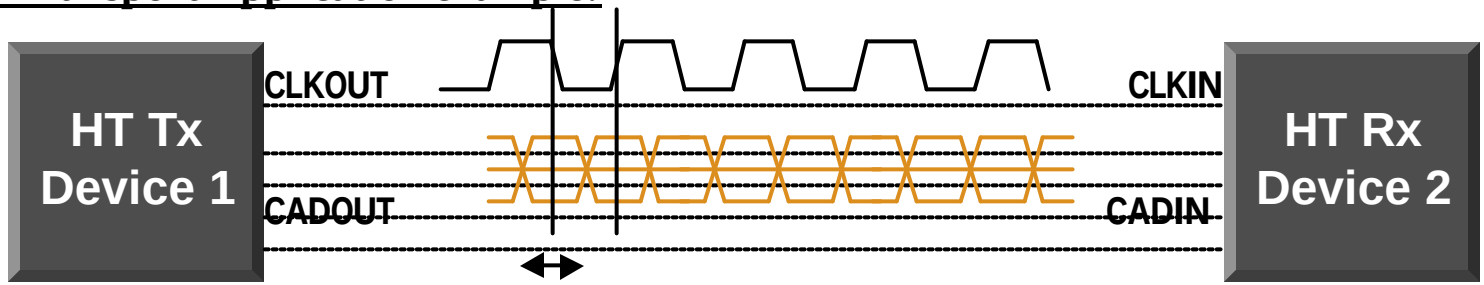


10 ps /div

53.8 ps p-p Jitter!

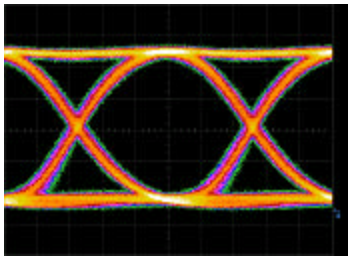
The Source Synchronous Test Challenge

HyperTransport Application example:

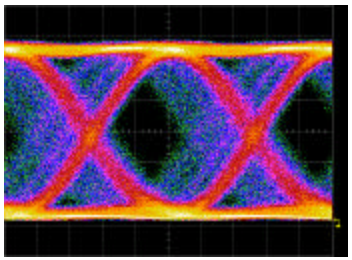


- CLKOUT shows Accumulated Phase Shift of PLL.
- CADOUT moves with phase shift.

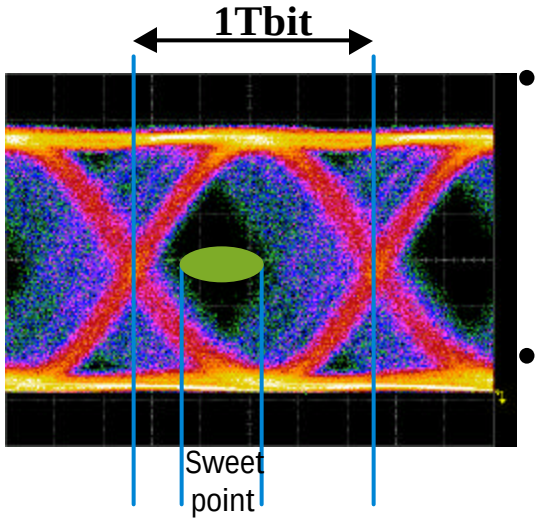
- **What does the HT receiver see?**
  - **Sampling Clock moves with shift**
  - **Data eye stays open**



- **What does a "standard" ATE see?**
  - **Sampling Clock is fixed**
  - **Data eye closes**



None Source Synchronous Tester



- **What is the minimum EPA a tester needs?**

$$t_{\pm EPA} \le \frac{\Delta t_{Bit} - \Delta t_{CumPhasErr} - \Delta t_{\mathrm{Pr}ocessM\,\mathrm{arg}in}}{4}$$

- **Calculation example with:**

1) **1UI = 800 Mbit Tbit = 1.25 ns**
2) **1UI = 1.6 Gbit Tbit = 625 ps**
& Cum Phase Error = +/-250ps
& Process Variation = +/- 50ps

1) $$t_{\pm EPA\_800\,Mbit} \le \frac{1.25ns - 500\,ps - 100\,ps}{4} = 162.5\,ps$$

2) $$t_{\pm EPA\_1.6Gbit} \le \frac{625\,ps - 500\,ps - 100\,ps}{4} = 6.25\,ps$$

Conclusion:

- Beyond the Gigabit you will need a tester which operates Source Synchronous

Summary

TEST LIST	*ATE NEEDS*	*COVERED*
Impedance Test (Input, Output)	DC Access	✓
Receiver Sensitivity Test	Level Accuracy & Resolution Low Swing capability	✓
Receiver Skew Insertion	Timing Accuracy & Resolution	✓
Transmitter Skew Measurements	Timing Accuracy, High Linearity	✓
Dynamic Transmitter Voltage Test	Level Accuracy, High Bandwidth	✓
Rise / Fall Time Measurements.	High Bandwidth, Resolution, Low Overdrive	✓
Eye Mask Test	High Bandwidth, Voltage & Timing Accuracy	✓
Jitter Test	Low System Jitter, All Others	✓
Source Synchronous Test	Source Synchronous Mode	✓
HV Production Solution	Full Integrated Solution, High Throughput	✓